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Patent

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Iiro Hietanen
Application No.	:	10/522,262
Filed	:	July 18, 2003
For	:	SEMICONDUCTOR STRUCTURE FOR IMAGING DETECTORS
Publication No.	:	US 2006/0097290 A1
Publication Date	:	May 11, 2006

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

THIRD PARTY SUBMISSION IN PUBLISHED APPLICATION UNDER 37 CFR §1.99

Dear Sir:

The references listed below (copies enclosed) are relevant to the above-referenced published application:

Entry Approved HH 7/24/06

U.S. PATENTS

Patent No.	Kind Code	Issue Date	Name of Patentee
4227942		1980-10-14	Hall
4626613		1986-12-02	Wenham et al.
4984358		1991-01-15	Nelson
5468652		1995-11-21	Gee
6836020	B2	2004-12-28	Cheng et al.

NON-PATENT LITERATURE DOCUMENTS

Cite No.	Description
1	E.M. CHOW, "Electrical Through-Wafer Interconnects and Microfabricated Cantilever Arrays Using Through-Wafer Silicon Etching," Thesis at Stanford University, 2001, 195 pages.
2	E.M. CHOW ET AL., "Process Compatible Polysilicon-Based Electrical Through-Wafer Interconnects in Silicon Substrates," Journal of Microelectromechanical Systems, Vol. 11, No. 6, December 2002, pages 631-640.

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3	C.H. CHENG ET AL., "An Efficient Electrical Addressing Method Using Through-Wafer Vias for Two-Dimensional Ultrasonic Arrays," 2000 IEEE Ultrasonics Symposium, pages 1179-1182.
4	C.H. CHENG ET AL., "Electrical Through-Wafer Interconnects with Sub-PicoFarad Parasitic Capacitance," IEEE Microelectromechanical Systems Conference, 2001, pages 18-21.
5	V. CHANDRASEKARAN ET AL., "Through-Wafer Electrical Interconnects for MEMS Sensors," Proceedings of 2001 ASME International Mechanical Engineering Congress and Exposition, Nov. 2001, pages 1-6.

Enclosed herewith is the required $180.00 fee for this submission as set forth in 37 CFR §1.17(p).

This submission is being filed within two months of the date of publication of the above-referenced published application and prior to the mailing of a Notice of Allowance, in accordance with 37 CFR §1.99(e). Also enclosed with this submission is a self-addressed postcard, in accordance with 37 CFR §99(f).

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LOCUST VALLEY NY 11560

Respectfully submitted,

Frederick M. Fliegel
Reg. No. 36,138

Date: July 10, 2006

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Application Serial No. 10/522,262
Filing Date ..... July 18, 2003
Inventor ..... Iiro Hietanen
Group Art Unit .....
Examiner .....
Title: Semiconductor structure for imaging detectors

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INFORMATION DISCLOSURE STATEMENT

(Use as many sheets as necessary)

Sheet 1 of 2

Complete if Known	
Application Number	10522262
Filing Date	2003-07-18
First Named Inventor	Iiro Hietenen
Art Unit	2811
Examiner Name	
Attorney Docket Number	800186US

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	1	US- 4227942	10-14-1980	Hall	
	2	US- 4626613	12-02-1986	Wenham et al.	
	3	US- 4984358	01-15-1991	Nelson	
	4	US- 5468652	11-21-1995	Gee	
	5	US- 6836020 B2	12-28-2004	Cheng et al.	
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FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3]-Number[4]-Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T[6]

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INFORMATION DISCLOSURE STATEMENT

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Sheet 2 of 2

Complete if Known	
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First Named Inventor	Iiro Hietenen
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NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	1	E.M. CHOW, "Electrical Through-Wafer Interconnects and Microfabricated Cantilever Arrays Using Through-Wafer Silicon Etching," Thesis at Stanford University, 2001, 195 pages.	
	2	E.M. CHOW ET AL., "Process Compatible Polysilicon-Based Electrical Through-Wafer Interconnects in Silicon Substrates," Journal of Microelectromechanical Systems, Vol. 11, No.	
	3	C.H. CHENG ET AL., "An Efficient Electrical Addressing Method Using Through-Wafer Vias for Two-Dimensional Ultrasonic Arrays," 2000 IEEE Ultrasonics Symposium, pages 1179-1182	
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	5	V. CHANDRASEKARAN ET AL., "Through-Wafer Electrical Interconnects for MEMS Sensors," Proceedings of 2001 ASME International Mechanical Engineering Congress and Exposition, Nov	

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1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.

United States Patent [19]

Hall

[11] **4,227,942**

[45] **Oct. 14, 1980**

[54] **PHOTOVOLTAIC SEMICONDUCTOR DEVICES AND METHODS OF MAKING SAME**

[75] Inventor: **Robert N. Hall, Schenectady, N.Y.**

[73] Assignee: **General Electric Company, Schenectady, N.Y.**

[21] Appl. No.: **32,117**

[22] Filed: **Apr. 23, 1979**

[51] Int. Cl.³ **H01L 31/06**

[52] U.S. Cl. **136/255**; 29/572; 136/256; 156/647; 156/657; 156/662; 148/179; 148/187; 357/30; 357/55; 357/68

[58] Field of Search ..... 136/89 CC, 89 SJ; 357/30, 55, 68; 29/572; 156/647, 657, 662; 148/179, 187

[56] **References Cited**

U.S. PATENT DOCUMENTS

3,020,412	2/1962	Byczkowski	250/211
3,150,999	9/1964	Rudenberg et al.	136/89
3,682,708	8/1972	Bennett	136/89
3,813,585	5/1974	Tarui et al.	357/41
4,046,594	9/1977	Tarui et al.	136/89 SJ
4,133,698	1/1979	Chiang et al.	136/89 SJ
4,135,950	1/1979	Rittner	136/89 SJ

OTHER PUBLICATIONS

E. Bassous, "Fabrication Process for Precise Control of Nozzle Dimensions", *IBM Tech. Disc. Bull*, vol. 20, pp. 2474–2479, (1977).

J. J. Loferski et al., "An Experimental Investigation Into the Feasibility of Higher Efficiency Silicon Solar Cells", *Conf. Record, 9th IEEE Photovoltaic Specialists Conf.*, (1972), pp. 19–26.

Primary Examiner—Aaron Weisstuch

Attorney, Agent, or Firm—Julius J. Zaskalicky; James C. Davis, Jr.; Marvin Snyder

[57] **ABSTRACT**

A solar cell which has high efficiency and which can be fabricated at low cost is described. The cell includes a semiconductor wafer with a front radiation-receiving surface which is entirely open and free of current conducting grids and also includes an array of interconnection paths which carry photocurrent from the front surface through the cell to metal electrodes on the rear surface of the cell.

19 Claims, 10 Drawing Figures

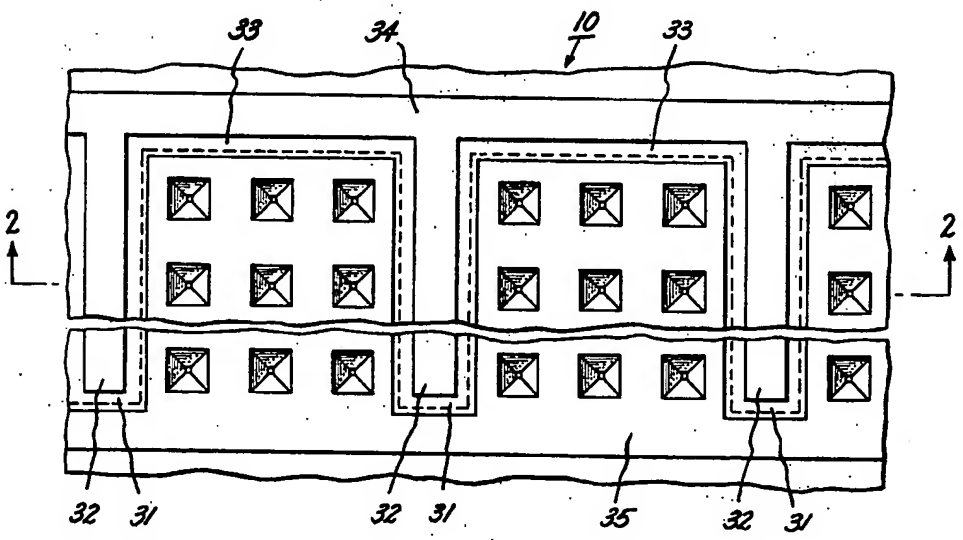


Fig. 1.

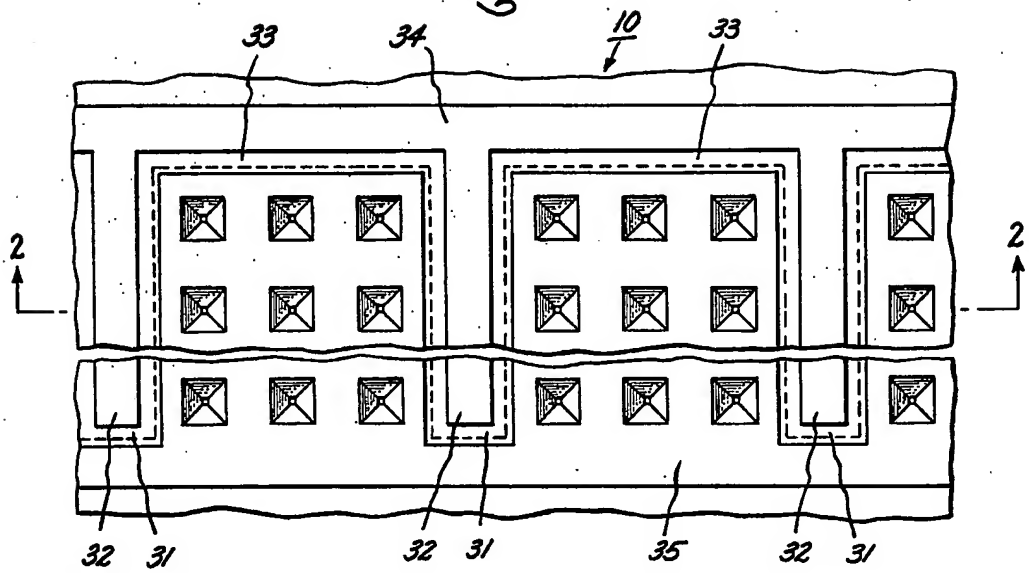


Fig. 2.

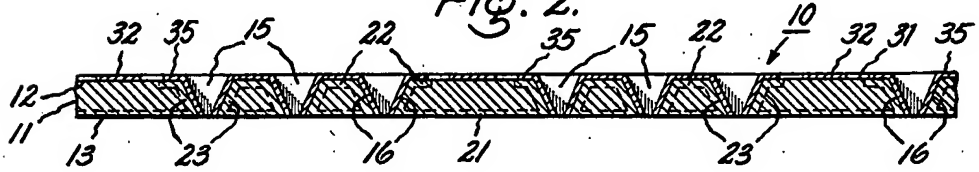


Fig. 3.

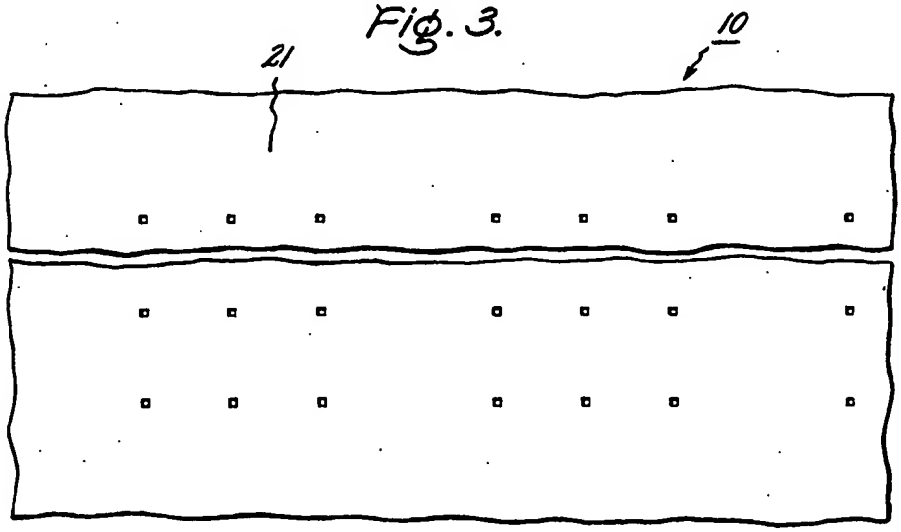


Fig. 4.

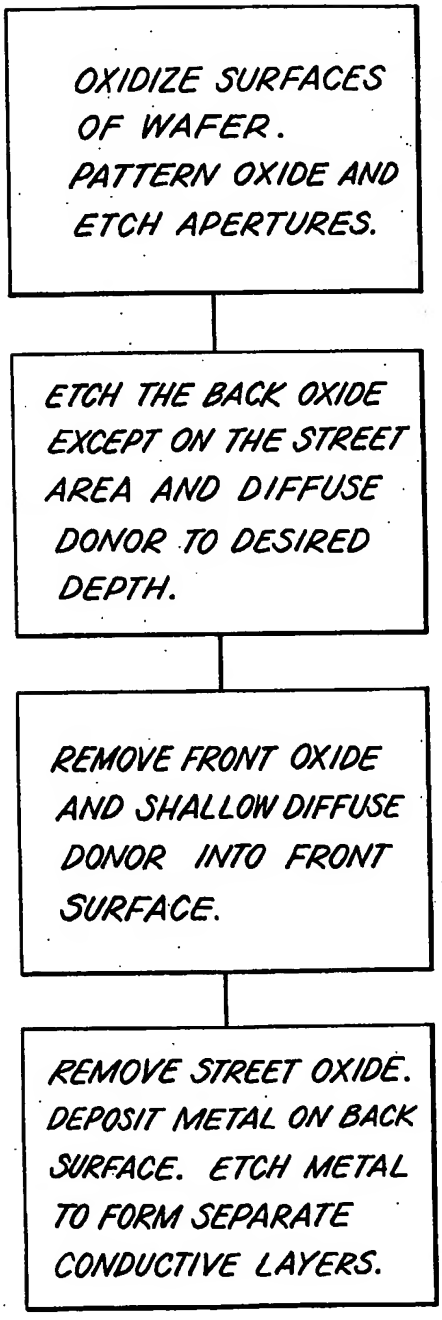


Fig. 5a.

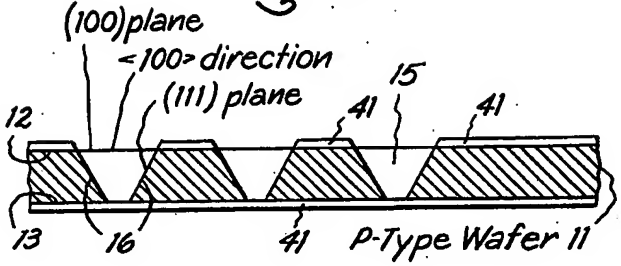


Fig. 5b.

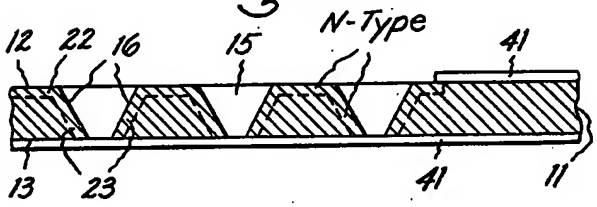


Fig. 5c.

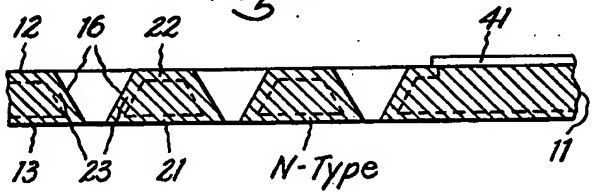


Fig. 5d.

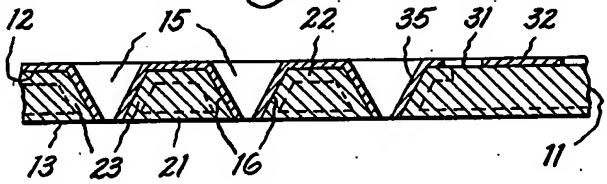


Fig. 6.

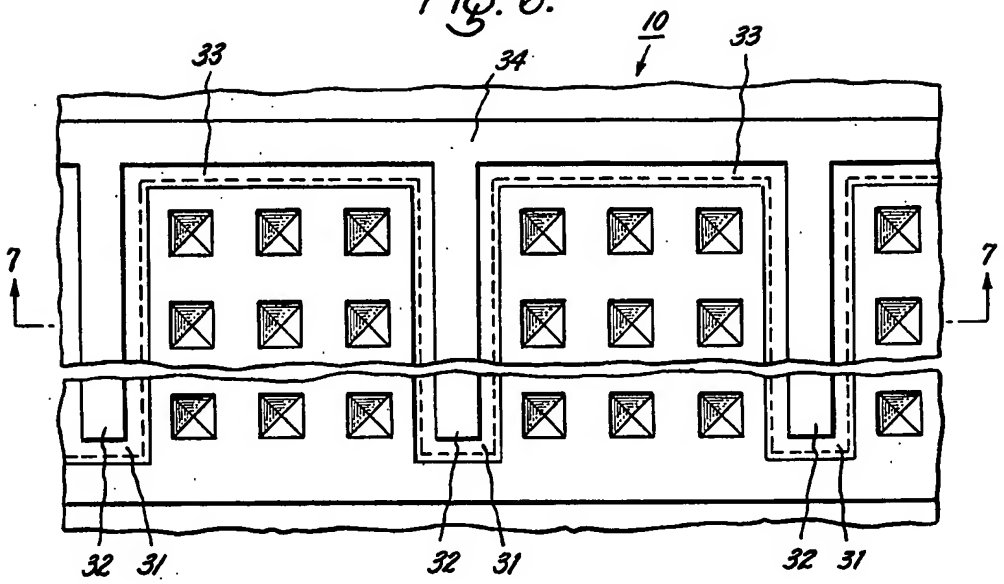


Fig. 7

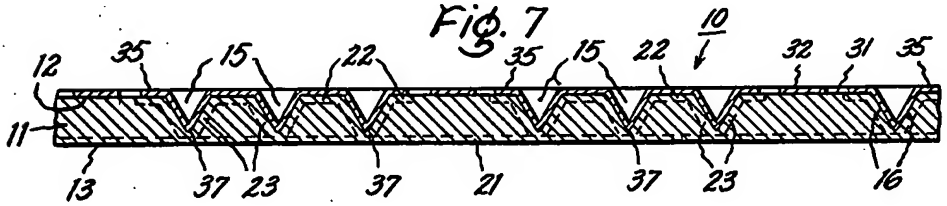


Fig. 8.

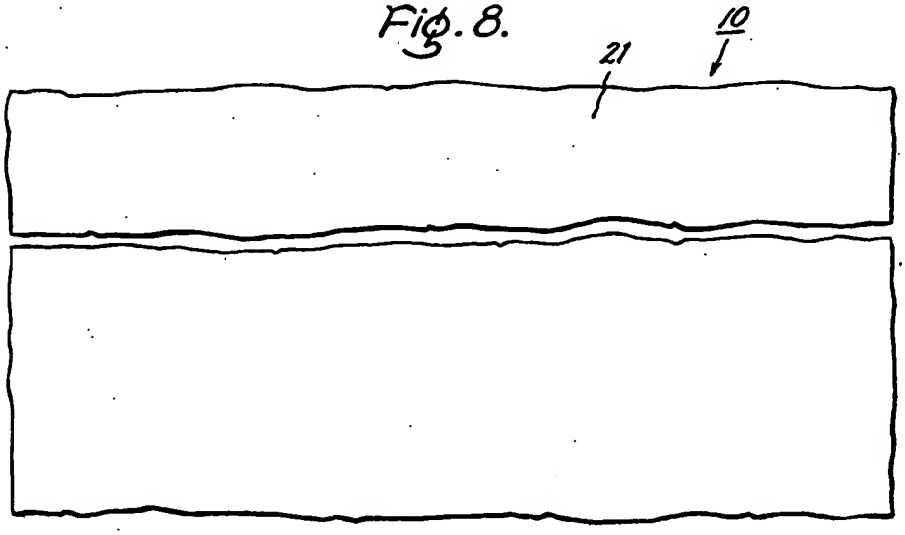


Fig. 9.

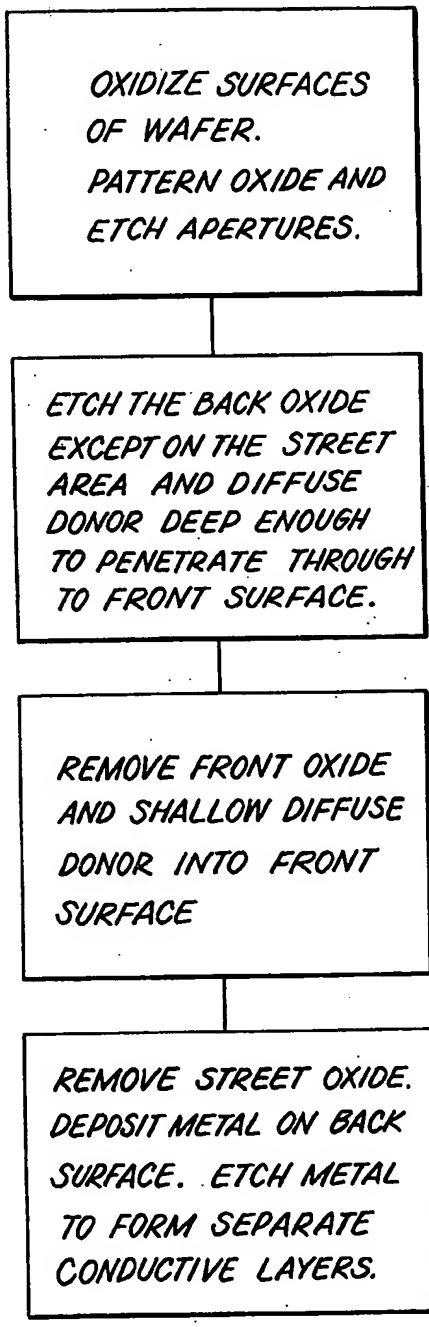


Fig. 10a.

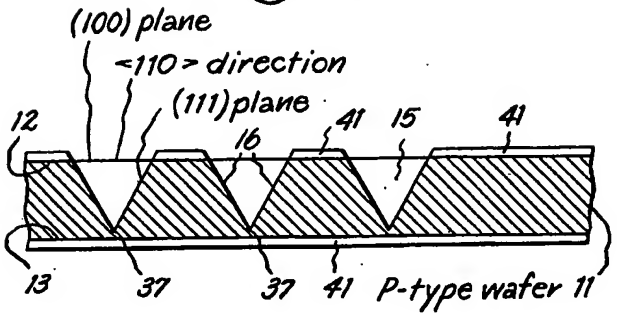


Fig. 10b.

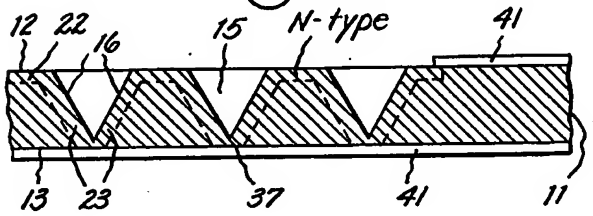


Fig. 10c.

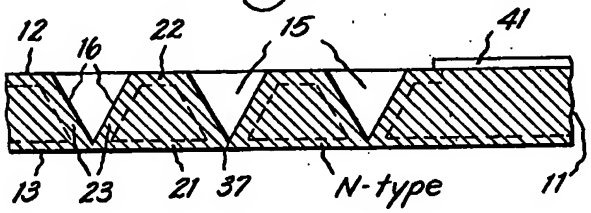
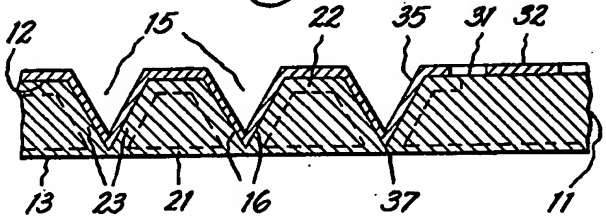


Fig. 10d



PHOTOVOLTAIC SEMICONDUCTOR DEVICES AND METHODS OF MAKING SAME

The present invention relates to photovoltaic semiconductor devices commonly referred to as solar cells and methods of making same.

An object of the present invention is to provide a photovoltaic semiconductor device having improved efficiency of conversion of optical radiation into electrical energy.

Another object of the present invention is to provide a relatively simple solar cell structure of planar form.

A further object of the present invention is to provide a relatively simple and low-cost method of fabricating photovoltaic semiconductor devices.

In carrying out the invention in one illustrative embodiment thereof there is provided a body of cubic symmetry monocrystalline semiconductor material of one conductivity type having a pair of opposite parallel major surfaces, each parallel to a (100) crystallographic plane of the body. A plurality of recesses are provided in the body, each extending from one of the major surfaces a uniform distance into the body. The sides of each of the recesses are in the form of quadrangular pyramids with the bases of the pyramids coplanar with the one major surface. Each of the sides of the recesses is parallel to a (111) plane of the body. A first thin region of opposite conductivity type is provided in the body adjacent the other major surface of the body. A second thin region of opposite conductivity type is provided in the body adjacent the one major surface of the body. A plurality of third thin regions of opposite conductivity type are provided in the body, each adjacent the sides of a respective one of the recesses. Each of the third thin regions contact the first and second thin regions. A first conductive layer is provided connected to the second and third thin regions of opposite conductivity type. A second conductive layer is provided connected to the one type conductivity region of the body over a portion of the one major surface thereof.

The novel features which are believed to be characteristic of the present invention are set forth with particularity in the appended claims. The invention itself, both as to its organization and method of operation, together with further objects and advantages thereof, may best be understood by reference to the following description taken in connection with the accompanying drawings wherein:

FIG. 1 is a plan view of a photovoltaic semiconductor device in accordance with one embodiment of the present invention showing the rear or electrode interconnection surface thereof.

FIG. 2 is a sectional view of the device of FIG. 1 taken along section lines 2—2 showing the internal structure thereof.

FIG. 3 is a bottom plan view of the device of FIG. 1 showing the front or radiation-receiving surface thereof.

FIG. 4 is a flow diagram of a method of fabricating the device of FIGS. 1–3 in accordance with the present invention.

FIGS. 5*a*–5*d* are schematic illustrations of vertical cross-sections of a body of monocrystalline silicon semiconductor material in the process of fabrication of the semiconductor device in accordance with the method of the flow diagram of FIG. 4.

FIG. 6 is a top plan view of a photovoltaic semiconductor device in accordance with another embodiment of the present invention showing the rear or electrode interconnection surface thereof.

FIG. 7 is a sectional view of the device of FIG. 6 taken along section lines 7—7 thereof showing the internal structure thereof.

FIG. 8 is a bottom plan view of the device of FIG. 6 showing the front or radiation-receiving surface thereof.

FIG. 9 is a flow diagram of a method of fabricating the device of FIGS. 6–8 in accordance with the present invention.

FIGS. 10*a*–10*d* are schematic illustrations of vertical cross-sections of a body of monocrystalline silicon semiconductor material in the process of fabrication of the semiconductor device in accordance with the method of the flow diagram of FIG. 9.

Referring now to FIGS. 1, 2 and 3 there is shown a photovoltaic semiconductor device 10 embodying the present invention. The device includes a body 11 or wafer of monocrystalline silicon semiconductor material of P-type conductivity, for example, 0.3 ohm-cm. The body 11 includes a pair of opposite parallel major surfaces 12 and 13, each parallel to a (100) crystallographic plane of the body. A plurality of recesses or apertures 15 are provided in the body 11 each extending from the major surface 12 through to the opposite major surface 13. Each of the recesses has four sides 16 of identical outline constituting the sides of a truncated quadrangular pyramid. The base of the pyramid is coplanar with the major surface 12 and the truncated surface of the pyramid is coplanar with the surface 13. Thus, each of the apertures 15 has a large opening in the plane of the major surface 12 and a small opening in the plane of the surface 13. A first thin region 21 of N-type conductivity is formed adjacent the major surface 13 of the body. A second thin region 22 of N-type conductivity is formed in the body adjacent the major surface 12. A plurality of third thin regions 23 of N-type conductivity are formed, each adjacent the sides 16 of the apertures 15. Each of the third thin regions 23 contact both the first thin region 21 and the second thin region 22.

The body 11 of P-type silicon semiconductor material may be doped with boron and have a concentration of activator atoms of about 10^{17} atoms per cubic centimeter, providing a resistivity of about 0.3 ohm-cm. The first, second and third thin regions 21, 22 and 23, respectively, of N-type conductivity may have a net activator concentration at the surface regions thereof of about 10^{20} atoms of phosphorous per cubic centimeter, providing a resistivity of about 0.001 ohm-cm. The thickness of the first thin region 13 is preferably less than a micron to enable a substantial portion of incident radiation to penetrate beyond the PN-junction formed adjacent the major face 13 and be absorbed in the body 11. The series resistance of the device 10 is dependent on the resistivity of the first thin region 13 and its thickness, and upon the size of the truncated ends of the pyramids and their separation. To lower the series resistance it is desirable to decrease the resistivity and increase the thickness of this thin region. However, such steps increase the absorption of radiation therein and also reduce the lifetime of minority carriers therein and thus result in reducing the efficiency of conversion of incident radiation into electrical output. The resistivity of the first thin region 13 is selected with attention to these considerations in accord with well-established solar cell

technology. The second and third thin regions of N-type conductivity preferably are substantially thicker, for example, of the order of 2 to 10 microns to provide low resistance and sufficient depth to enable metallic films or layers to be bonded thereto without destroying the integrity of the PN-junctions they form with the body 11 of P-type conductivity.

The apertures 15 are shown organized in a regular pattern consisting of sets or groups of apertures. In the plane 12 the apertures appear as squares. Each group of squares consists of three columns and a plurality of rows. The squares in a row are shown equally spaced and also the squares in a column are shown equally spaced. In this example, the spacing between squares in a row and also the spacing between squares in a column is shown equal to the dimension of a side of a square although such equality is not essential. Adjacent columns of successive sets or groups of squares are spaced apart by a distance equal to three times the dimension of a side of a square. An area 31 of the major surface 12 extending in the column direction does not include the second thin region 22 of N-type conductivity and is referred to as a street area. Also an area 33 of the major surface strip extending in the row direction spaced above the first row of squares does not include the second thin region of N-type conductivity and is referred to as an avenue area. These street and avenue areas are of P-type conductivity and enable ohmic or low impedance connections to be made to the body 11 to constitute one of the current carrying electrodes of the device. As shown in FIGS. 1 and 2, conductive fingers 32 extending in the column direction are bonded to the street areas 31. The conductive fingers 32 are joined in the conductive bus 34 bonded to the avenue area 33 of the surface 12 to constitute the second electrode of the device. The first electrode 35 of the device is provided by a conductive layer 35 bonded to the second and third regions of N-type conductivity type. The conductive layer 35 is constituted of wide fingered conductors extending in the column direction and each overlying a respective set or group of apertures and bonded thereto. The wide fingered conductors are interconnected at the side thereof remote from the conductive bus 34.

Preferably, the body 11 of semiconductor material is not so thin that it would be difficult to handle in the fabrication thereof and on the other hand should not be so thick that carriers generated by incident radiation would recombine in the body before being collected by an adjacent PN-junction. Conveniently, the body may be 10 mils thick. In accord with the selective etching method herein described for forming apertures 15, with such a starting dimension each of the square openings of the body of the aperture would be about 15 mils to provide the structure shown in FIGS. 1, 2 and 3. The side of a square opening is made slightly greater than the thickness of the body multiplied by $\sqrt{2}$.

Reference is now made to FIGS. 4 and 5*a*–5*d*, which illustrate a manner of fabrication of the devices of FIGS. 1-3 in accordance with another aspect of the present invention to provide a solar cell constituted of a body of P-type conductivity. A piece of monocrystalline silicon is cut from an ingot of P-type conductivity to provide a wafer 11 having a pair of opposite parallel major surfaces, each parallel to a (100) crystallographic plane of the wafer. The ingot of P-type conductivity has been doped with a suitable doping agent, such as boron, to provide a suitable resistivity to the wafer, for example, 0.3 ohm-cm. The major surfaces of the wafer are etched to provide a wafer about 10 mils thick with a pair of smooth planar surfaces 12 and 13. After standard cleaning, the wafer is oxidized in steam for a time and temperature to provide a thin layer of silicon dioxide 41 about 1 micron thick on each of the major surfaces 12 and 13 of the wafer. The silicon dioxide layer 41 overlying the back or rear side 12 of the wafer is patterned using conventional photoresist masking and etching techniques to provide a pattern of square openings therein exposing the major surface 12. The square openings are arranged into groups, each group having three columns and a plurality of rows. The squares in a row are spaced from an adjacent square by a distance equal to a side of the square and similarly the squares in a column are spaced from an adjacent square by the distance of a side of the square. Both the column axis and the row axis of squares are aligned parallel to a $<110>$ crystallographic direction of the wafer in the surface 12. Each group of square openings is separated in the row direction from an adjacent group of square openings by wide areas of silicon dioxide without openings and overlying the portion of the major surface 12, referred to as the street area. For a wafer 10 mils in thickness the sides of the square openings are made 15 mils wide so that when the silicon exposed by the square openings is anisotropically etched, as will be described below, an aperture of pyramidal outline extending to the opposite major surface 13 will be formed in which the sides of the aperture are parallel to (111) planes of the wafer which are oriented at 54.7 degrees with respect to the surface 12. After cleaning, the wafer is immersed in a suitable anisotropic etchant, such as an etchant consisting of approximately 3 parts by volume of a solution of 45% potassium hydroxide and 1 part by volume of isopropyl alcohol, for a sufficient period of time to cause etching action to occur into the portions of the wafer exposed by the square openings. Ultrasonic agitation of the etchant facilitates the etching action. The apertures 15 formed by the etching action extend to the opposite surface 13. The apertures are in the form of quadrangular pyramids the bases of which are squares in the surface 12 as shown in FIG. 5*a*, and also in FIGS. 1, 2 and 3. Next, the silicon dioxide layer 41 overlying the street areas 31 and avenue areas 32 and also the silicon dioxide layer overlying the front surface 13 of the wafer are covered with a protecting wax.

The wafer is then etched in a buffered hydrofluoric acid etchant to remove the portion of silicon dioxide layer 41 on the back or rear surface 12 not covered with wax. After cleaning, a donor such as phosphorous is diffused into the exposed surfaces 12 and 16 of the wafer to form the second thin region 22 and the third thin regions 23 in the wafer about 2 to 10 microns thick and of relatively low resistivity, as shown in FIG. 5*b*. This step may be an open tube diffusion step in which a phosphosilicate glass is deposited on the exposed surface of wafer and thereafter diffused at a temperature for a sufficient time to provide the desired depth and resistivity for the second and third thin regions.

While protecting the silicon dioxide layer 41 overlying the street and avenue areas 31 and 33 by covering these areas with wax, the silicon dioxide layer on the front surface 13 is removed in a suitable etchant such as buffered hydrofluoric acid. Thereafter, the wafer 11 is subjected to a diffusion step in which phosphorous is diffused into the front surface 13 to a shallow depth to provide the first thin region 21 of the device of FIGS. 1,

2 and 3, for example, less than 1 micron thick and of low resistivity. The open tube diffusion process mentioned above could also be utilized to provide this first thin region 21. The time and temperature utilized is such as to provide the desired depth and resistivity for this first thin region 21. In the next step, the silicon dioxide layer overlying the street and avenue areas of the wafer and the phospho-silicate glass overlying the remaining portions of the rear surface 12, the sides 16 of the apertures 15 and the front surface 13 are removed by etching in a suitable etch such as buffered hydrofluoric acid, and the wafer is cleaned. Thereafter, the rear surface 12 and also the surfaces 16 of the apertures 15 are metallized with a metal such as aluminum to a suitable thickness, for example, 2 microns. The aluminum layer is then selectively etched using photoresist masking and etching techniques well-known in the art to provide a first conductive layer 35 making contact to the second thin region 22 of N-type conductivity adjacent the major surface 12 and to the third thin region 23 of N-type conductivity adjacent the sides of the apertures and a second conductive layer 32 and 34 overlying the street and avenue areas and making contact to the P-type wafer 11 of semiconductor material in the rear surface thereof.

Reference is now made to FIGS. 6, 7 and 8 illustrating another embodiment in accordance with the present invention similar to the embodiment of FIGS. 1, 2 and 3. The elements of the device of FIGS. 6, 7 and 8 identical to the device of FIGS. 1, 2 and 3 are identically designated. The essential difference in the device of this figure is that the recesses 15 stop at a point 37 a short distance from the front surface 13. This distance is less than the thickness of the third thin regions 23 of opposite conductivity type adjacent the sides 16 of the recesses so that the third thin regions 23 connect with the first thin region 21. This result is obtained, as will be pointed out in connection with FIGS. 8, 9 and 10, by setting the dimension of a side of the square openings equal to slightly less than the thickness of the body multiplied by $\sqrt{2}$.

Reference is now made to FIGS. 9 and 10*a*–10*d* which illustrate a manner of fabrication of the device of FIGS. 6–8 in accordance with another aspect of the present invention. The method illustrated in connection with FIGS. 9 and 10*a*–10*d* is similar to the method illustrated in connection with FIGS. 4 and 5*a*–5*d* except that third thin regions 23 are made thicker and the sides of the square openings are made equal to less than the thickness of the wafer multiplied by $\sqrt{2}$ so that the recesses 15 depicted in FIG. 10*a* extend into the wafer to points 37 a short distance from the front face 13. The predetermined distance between the apex 37 of the recess and the front surface 13 is made less than the thickness of the third thin region 23 of opposite conductivity type so that in the process of formation of the various first, second and third thin regions in the wafer, the third thin region contacts the first thin layer and provides a low resistance connection thereto. If it is assumed that the third thin regions 23 are 40 microns thick, the distance between point 37 and the front surface 13 could be set equal to about 20 microns. Apertures extending to within 20 microns of the front surface 12 would be obtained by starting with square openings having sides equal to the thickness of the wafer less 20 microns multiplied by $\sqrt{2}$. For a 10 mil wafer, the sides of the squares would be 13 mils. The anisotropic etching of the wafer would stop when the point 37 is reached representing the intersecting of the (111) planes of the wafer.

The photovoltaic devices of the present invention have a number of features which provide increased efficiency over conventional photovoltaic devices. The front or radiation-receiving surface is free of any metal grid thereby eliminating shadowing losses. The absence of grid metallization on the front surface eliminates the degradation of the thin front-surface PN-junction caused by the overlying metal in conventional devices. The PN-junction adjacent the rear surface of applicant's device is made deeper to avoid this problem. Series resistance is substantially reduced. The spreading resistance in the first thin region 21 of FIGS. 1–3, adjacent the front surface around the small holes therein is much less than that of an array of parallel line contacts of equal area, and the ohmic drop along such lines themselves is eliminated. Also, metallization layers on the second thin region 22 and third thin region 23 provide a low impedance path to the first thin region 21 as well as the second thin region 23 and the third thin region 23. Also, current is collected at both the front and rear surfaces of the devices thereby reducing carrier recombination losses therein. The (100) crystallographic orientation that is required for the formation of the pyramidal recesses also permits the creation of a textured front surface which reduces reflection loss. Also, anti-reflection layers may be applied to the front surface to further reduce reflection losses. The performance of the device is independent of the area or diameter of the semiconductor body utilized in the device. As the device has a planar front, it is also easier to assemble in modules.

In accordance with the present invention a relatively simple and low-cost method of fabricating solar cells is also provided. Only one photoresist operation, which does not involve registration with a previous pattern, is required. No high-definition metallization is used. All patterning is on the rear surface of the semiconductor wafer so there is no conflict with having a textured front surface.

While in the devices described in connection with FIGS. 1–3 and FIGS. 6–8, the apertures 15 have square openings in the plane of major surface 12, rectangular openings could have been utilized, if desired, to provide pyramidal apertures with rectangular bases. Also, while the square openings were produced with etch masks having square openings, they could as well have been produced with etch masks with circular openings. In the latter case anisotropic etching would cause etching to occur with respect to each circular opening over a surface region bounded by square openings having sides parallel to <110> directions in which the circular opening is inscribed. The resultant aperture would be a quadrangular pyramid with each of the sides thereof parallel to a (111) plane of the semiconductor material.

While in the fabrication of the devices shown in FIGS. 1–3 and FIGS. 6–8, the second thin region 22 and the third thin region 23 were formed first by a first diffusion step and thereafter the first thin region 21 adjacent the front surface 13 was formed by a second diffusion, all of these regions may be formed at the same time by initially ion implanting more slowly diffusing donor activators such as arsenic in the silicon dioxide layer 41 overlying the front surface 13 and therefore enable the formation of the first thin region 21 while the second thin region 22 and third thin region 23 are being formed as previously formed.

While in the device of FIGS. 1, 2 and 3, and the device of FIGS. 6, 7 and 8 only several groups of apertures have been shown, as many such groups as desired may be included extending in both the row and column directions limited only by the size of the wafer on which such apertures are formed.

While each of the groups shown include a row of three apertures, the number of apertures in a row may be increased or decreased, as desired. Also the spacing between adjacent apertures in a group may be changed as desired, to increase or decrease the density of apertures in the wafer. Of course, different sizes of apertures would be used with wafers of different thicknesses. The preferred choice among the variants is determined by wafer resistivity and solar intensity.

While the invention has been illustrated in connection with devices using silicon semiconductor material, other monocrystalline semiconductor materials of cubic symmetry, such as germanium and the Group III-Group V compound semiconductor materials may be utilized in accordance with the present invention. The utilization of such materials would require alteration in the details of the steps of fabrication of devices of these semiconductor materials in accordance with their respective technologies.

While the device has been illustrated in connection with a body or wafer of semiconductor material of P-type conductivity, it will of course be understood that N-type semiconductor material may as well be used. Use of such material would of course require the first, second and third thin regions to be of P-type conductivity.

While the invention has been described in specific embodiments, it will be understood that modifications such as those described above, may be made by those skilled in the art and it is intended by the appended claims to cover all such modifications and changes as fall within the true spirit and scope of the invention.

What I claim as new and desire to secure by Letters Patent of the United States is:

1. A photovoltaic device comprising

a body of cubic symmetry monocrystalline semiconductor material of one conductivity type having a pair of opposite parallel major surfaces, each parallel to a (100) crystallographic plane of said body,

a plurality of recesses in said body, each in the form of a quadrangular pyramid with the base of the pyramid coplanar with one of said pair of major surfaces and extending a uniform distance into said body, each of the sides of the recesses being parallel to a (111) plane of said body of monocrystalline semiconductor material,

a first thin region of opposite conductivity type in said body along the other of said pair of major surfaces of said body,

a second this region of opposite conductivity type in said body along said one major surface of said body,

a plurality of third thin regions of opposite conductivity type, each in said body along the sides of said recesses, each of said third thin regions contacting said first and second thin regions,

a first conductive layer connected to said second and third thin regions of opposite conductivity type,

a second conductive layer connected to said one type conductivity region of said body over a portion of said one major surface.

2. The device of claim 1 in which said monocrystalline cubic symmetry semiconductor material is selected from the class of silicon and germanium.

3. The device of claim 1 in which said monocrystalline cubic symmetry semiconductor material is silicon.

4. The device of claim 1 in which each of said recesses is an aperture extending from said one major surface to said other major surface.

5. The device of claim 1 in which each of said recesses extends from said one major surface to a point located a small predetermined distance from said other major surface.

6. The device of claim 1 in which said recesses are arranged in a regular pattern in said body.

7. The device of claim 3 in which said first thin region is less than one micron thick.

8. The device of claim 3 in which said first thin region is substantially thinner than said second and third thin regions.

9. The device of claim 3 in which said portion of said one major surface includes areas spaced at intervals therealong, said second conductive layer being bonded on said areas.

10. A method of making a photovoltaic device comprising

providing a substrate of cubic symmetry monocrystalline semiconductor material of one conductivity type having a pair of parallel major surfaces, each parallel to a (100) crystallographic plane of said monocrystalline semiconductor material,

providing a first etch mask over one of said pair of major surfaces and a second etch mask over the other of said pair of major surfaces,

forming in said first etch mask a plurality of first openings to expose areas in a first portion of said one major surface, each first opening being identical in form and being bounded by two pairs of parallel opposed edges in said one major surface, each of said pairs of edges being substantially parallel to a respective <110> direction in said one major surface, each pair of parallel edges of each first opening being spaced apart by a distance slightly greater than the distance between said major surfaces multiplied by $\sqrt{2}$,

etching the exposed areas of said substrate with an anisotropic etchant to form a plurality of apertures each in the form of a quadrangular pyramid with the base of the pyramid being coplanar with said one major surface and extending from said one major surface to said other major surface to form a second opening therein substantially smaller than a respective one of said first openings, each of the sides of said apertures being parallel to a (111) plane of said monocrystalline semiconductor material.

removing said first etch mask at least from said first portion of said one major surface,

introducing a first dopant of opposite conductivity type into said other major surface to form a first thin region of opposite conductivity type in said substrate along said other major surface,

introducing a second dopant of opposite conductivity type into said first portion of said major surface to form a second thin region of opposite conductivity type in said substrate along said first portion of said one major surface;

introducing a third dopant of opposite conductivity type into the sides of said apertures to form third

thin regions of opposite conductivity type in said substrate along the sides of said apertures,

stripping said one major surface, and said other major surface of overlying layers of masking material,

depositing a layer of conductive material on said one major surface and the sides of said apertures,

patterning said conductive layer to provide a first electrode contacting said regions of opposite conductivity type adjacent said first portion of said one major surface and the sides of said apertures and a second electrode contacting said substrate of one conductivity type at another portion of said one major surface.

11. The method of claim **10** in which said first, second and third dopants are introduced into said substrate by diffusion.

12. The method of claim **10** in which said first dopant, said second dopant, and said third dopant are introduced simultaneously into said substrate to form simultaneously said first thin region, said second thin region and said third thin regions.

13. The method of claim **10** in which said second and third dopants are introduced into said substrate to form said second and third thin regions and thereafter said first dopant is introduced into said substrate to form said first thin regions.

14. The method of claim **10** in which each of said first openings are squares.

15. A method of making a photovoltaic device comprising

providing a substrate of cubic symmetry monocrystalline semiconductor material of one conductivity type having a pair of parallel major surfaces, each parallel to a (100) cyrstallographic plane of said monocrystalline semiconductor material,

providing a first etch mask over one of said pair of surfaces and a second etch mask over the other of said pair of major surfaces,

forming in said first etch mask a plurality of openings to expose areas in a first portion of said one major surface, each opening being identical in form and being bounded by two pairs of parallel opposed edges in said one major surface, each of said pairs of edges being substantially parallel to a respective <110> direction in said one major surface, each pair of parallel edges of each opening being spaced apart by a distance slightly less than the distance between said major surfaces multiplied by $\sqrt{2}$,

etching the exposed areas of said substrate with an anisotropic etchant to etch a plurality of recesses each in the form of a quadrangular pyramid with the base of the pyramid being coplanar with said one major surface and the apex thereof being located a small predetermined distance from said other major surface, each of the sides of said apertures being parallel to a (111) plane of said monocrystalline semiconductor material,

removing said first etch mask at least from said first portion of said one major surface,

introducing a first dopant of opposite conductivity type into said other major surface to form a first thin region of opposite conductivity type in said substrate along said other major surface,

introducing a second dopant of opposite conductivity type into said first portion of said one major surface to form a second thin region of opposite conductivity type in said substrate along said first portion of said one major surface,

introducing a third dopant of opposite conductivity type into the sides of said recesses to form third thin regions of opposite conductivity type in said substrate along the sides of said recesses, the thickness of said third thin region being greater than said small predetermined distance,

stripping said one major surface and said other major surface of overlying layers of masking material,

depositing a layer of conductive material on said one major surface and the sides of said recesses,

patterning said conductive layer to provide a first electrode contacting said regions of opposite conductivity type adjacent said first portion of said one major surface and the sides of said recesses and a second electrode contacting said substrate of one conductivity type at another portion of said one major surface.

16. The method of claim **15** in which said first, second and third dopants are introduced into said substrate by diffusion.

17. The method of claim **15** in which said first dopant, said second dopant, and said third dopant are introduced simultaneously into said substrate to form simultaneously said first thin region, said second thin region and said third thin regions.

18. The method of claim **15** in which said second and third dopants are introduced into said substrate to form said second and third thin regions and thereafter said first dopant is introduced into said substrate to form said first thin regions.

19. The method of claim **15** in which each of said openings are squares.

* * * * *

United States Patent [19]

Wenham et al.

[11] **Patent Number: 4,626,613**

[45] **Date of Patent: Dec. 2, 1986**

[54] **LASER GROOVED SOLAR CELL**

[75] Inventors: **Stuart R. Wenham; Martin A. Green, both of Sydney, Australia**

[73] Assignee: **Unisearch Limited, Kensington, Australia**

[21] Appl. No.: **683,505**

[22] Filed: **Dec. 19, 1984**

[30] **Foreign Application Priority Data**

Dec. 23, 1983 [AU] Australia PG3004

[51] **Int. Cl.**[4] **H01L 31/06; H01L 31/18**

[52] **U.S. Cl.** ..... **136/255; 29/572; 29/580; 29/583; 156/643; 156/644; 156/647; 219/121 LL; 219/121 LN; 357/20; 357/30; 357/52**

[58] **Field of Search** ..... 29/572, 580, 583; 219/121 LH, 121 LJ, 121 LK, 121 LL, 121 LN; 136/255, 256; 357/30, 20, 52; 156/643, 644, 647

[56] **References Cited**

U.S. PATENT DOCUMENTS

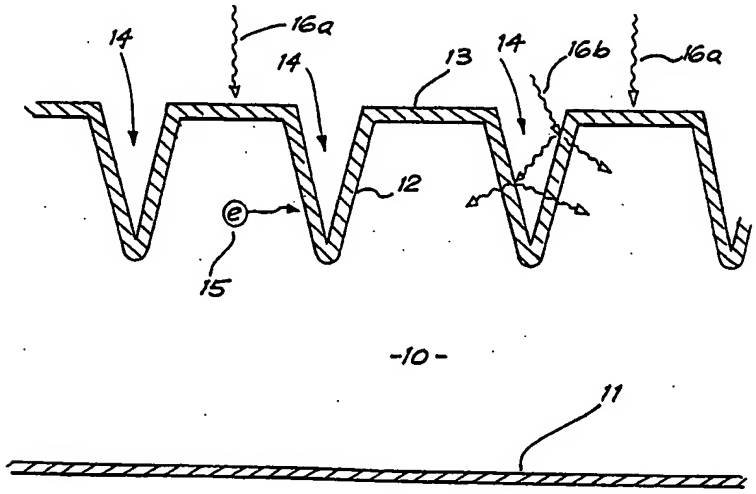
3,150,999	9/1964	Rudenberg et al.	136/256
3,278,337	10/1966	Gault	136/255
4,044,222	8/1977	Kestenbaum	219/121 LM
4,081,289	3/1978	Campbell, III	136/246
4,348,254	9/1982	Lindmayer	156/647
4,352,948	10/1982	Kaplow et al.	136/249 MS
4,409,423	10/1983	Holt	136/255
4,427,839	1/1984	Hall	136/255

Primary Examiner—Aaron Weisstuch

[57] **ABSTRACT**

Grooved solar cells are manufactured by scribing the surface of the substrate with a laser scribing tool, and optionally etching the surface to more accurately determine the surface profile, before performing the remainder of the processing steps involved in the production of the solar cell. Top contact shading is avoided by providing holes through the substrate which allow connection to the top layer of the cell to be made from the back of the cell. Resistance to radiation is improved by providing a cell which is grooved on the top and bottom surfaces, the grooves of the bottom surface being spaced between the grooves on the top surface to allow the formation of a relatively thin cell structure. Top layer sheet resistivity is also varied to allow improved efficiency while maintaining the series resistance of the cell substantially unaltered.

7 Claims, 17 Drawing Figures



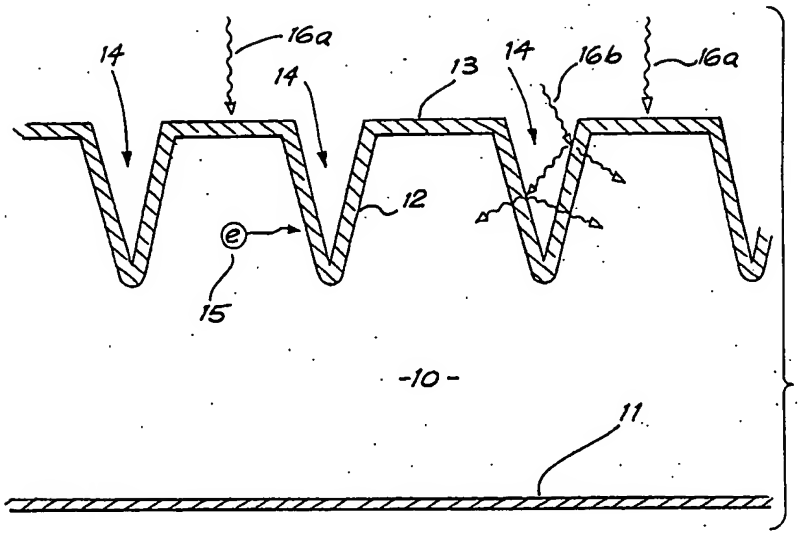


FIG. 1

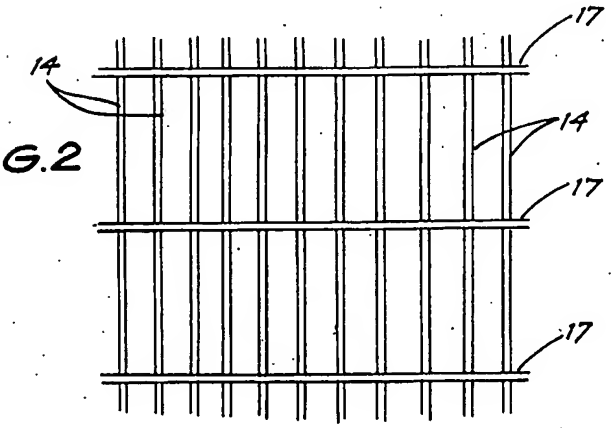


FIG. 2

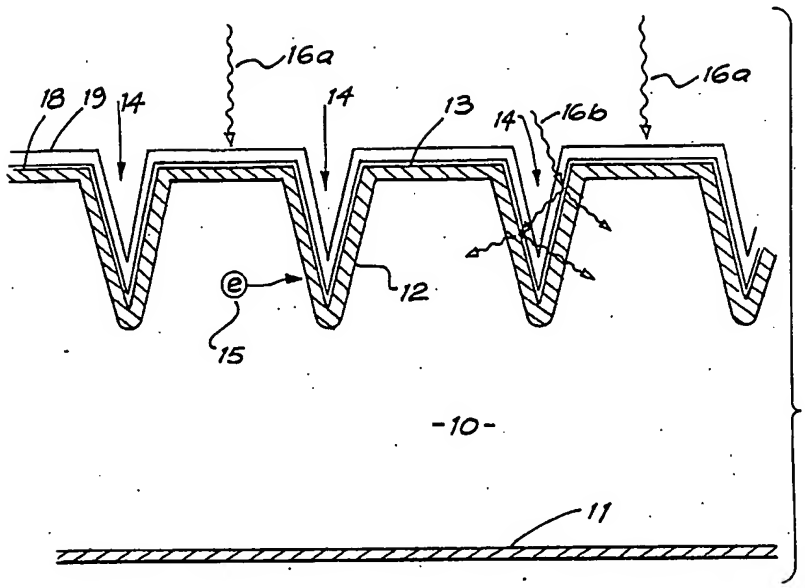


FIG. 3

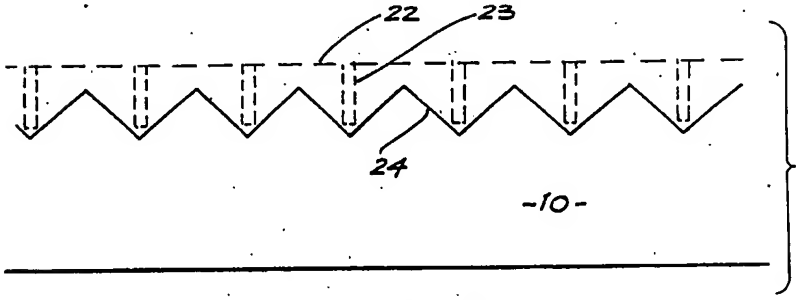


FIG. 4

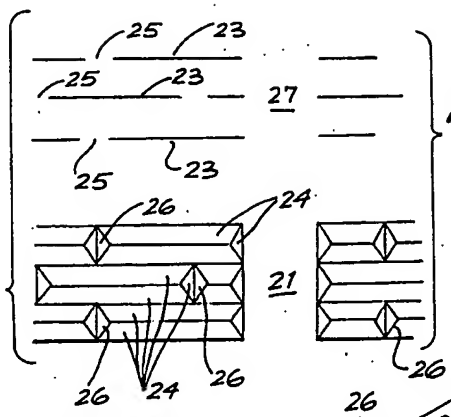
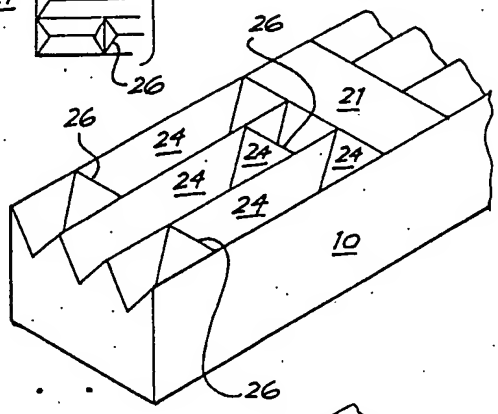


FIG. 5a

FIG. 5b

FIG. 5c



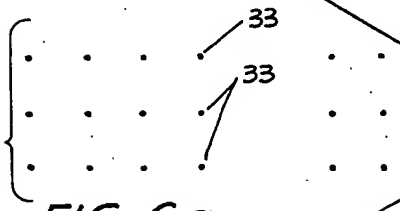


FIG. 6a

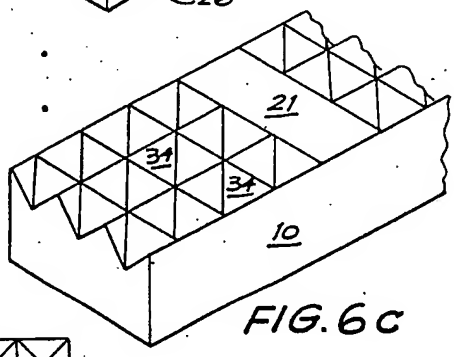


FIG. 6c

FIG. 6b

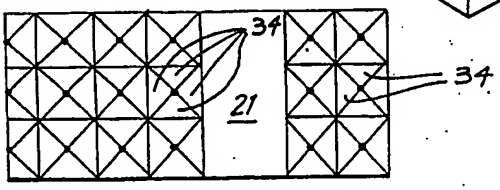


FIG. 7a

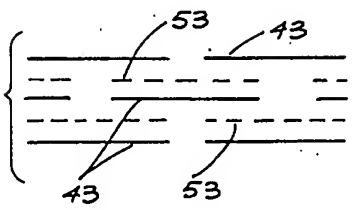
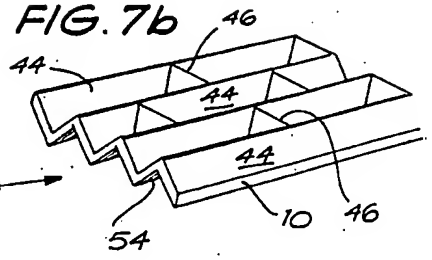


FIG. 7b



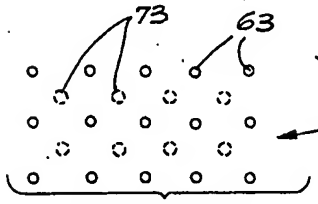


FIG. 8a

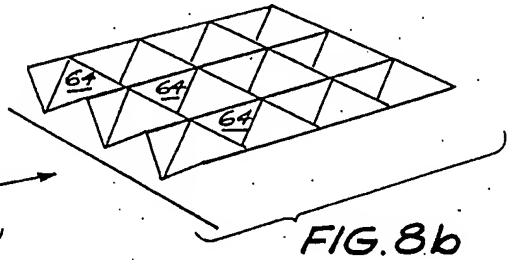
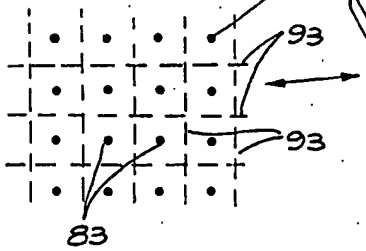


FIG. 8b

FIG. 9a



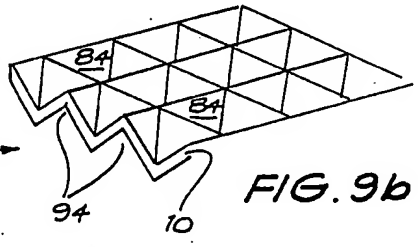
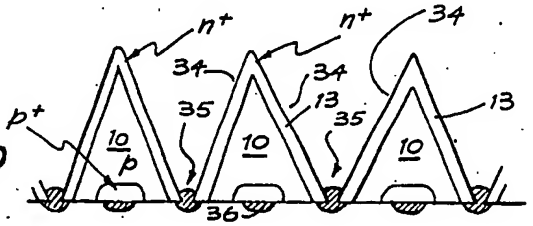


FIG. 9b

FIG. 10



LASER GROOVED SOLAR CELL

The present invention relates to improvements in the fabrication of solar cells whereby the structure of the cell facilitates collection of photon generated minority carriers from deep within the wafer substrate.

Long wavelength light striking a photocell will penetrate much further into the cell than shorter wavelength light, on average, before being absorbed and therefore minority carriers generated by photons of long wavelength energy must travel much further before being collected by the rectifying junction of the cell. As a result, the chances of a minority carrier resulting from a long wavelength photon, being collected before recombination occurs are greatly reduced over those of a minority carrier resulting from a shorter wavelength photon. This effect is even more pronounced in solar cells used in space, due to the radiation damage which is caused to a solar cell in this environment, and which results in a reduction in minority carrier life times.

In an attempt to overcome the effects of reduced minority carrier life time in the space environment, prior art solar cells have been produced wherein a plurality of grooves were chemically etched into the surface of the substrate prior to the formation of the rectifying junction of the cell, such that the junction provided within the grooves penetrates deep into the bulk of the substrate to aid in the collection of minority carriers formed in the bulk regions.

However, while the formation of grooves in the substrate provides an improvement in short circuit current densities, complications associated with the chemical etching step make this solution too expensive to be of practical use, particularly in the case of mass produced cells for terrestrial use.

A laser scriber has previously been used to separate cells formed on a common wafer, by scribing a groove between a pair of adjacent cells and then breaking the wafer along the scribe line in a similar manner to that used when cutting glass or ceramic tiles. Lasers have also been used to isolate doped regions of a substrate by cutting or drilling an opening between the two adjacent regions to be isolated, however, it has not previously been considered feasible to use lasers in the processing of the active regions of semiconductor devices, due to the damage to the crystal structure caused by the laser.

A first aspect of the present invention relies upon the unexpected result that grooves scribed in the surface of a substrate by way of a laser scriber do not cause a significant deleterious effect upon the solar cell subsequently formed on the substrate, due to crystal damage caused by the laser, but to the contrary, the crystal damage provides gettering sites to which impurities in the substrate migrate during subsequent high temperature processing, thereby enhancing the performance of the solar cell by increasing the life time of minority carriers in the bulk of the substrate.

It has also been found that grooving of the surface of the cell enhances the anti-reflective properties of the cell, as light falling within the grooved area, if it is not initially absorbed by the cell, will be reflected onto another surface of the groove, thereby increasing the possibility of absorption. In order to escape from the grooved area, a photon will need to be reflected several times within the groove, and therefore the probability of escape is low.

The provision of grooves in the substrate also increases greatly the area of the cell junction and additionally provides the possibility of having differing sheet resistivities in the top layer of the cell, with a high resistivity in the region between the grooves to enhance the photovoltaic effect and a lower resistivity within the grooves to decrease the series resistance of the cell and to allow the wider spacing of the contact fingers used to conduct current from the top layer.

According to a first aspect, the present invention consists in a method of manufacturing solar cells, said method comprising the steps of scribing a pattern of holes or grooves in a surface of a semiconductor substrate with a laser scriber and subsequently forming a rectifying junction on said surface, said junction extending into said holes or grooves.

Preferable embodiments of the invention achieve a plurality of parallel grooves or a regular pattern of holes by scribing the surface of the substrate using a laser scriber adapted to simultaneously scribe a repeating pattern of grooves or holes.

In a preferred embodiment of the invention, a chemical etching step is employed between the step of laser scribing and the step of forming the rectifying junction, such that precise control of the shape of holes and grooves is achieved.

Some embodiments of the invention will also make use of holes bored through the substrate during the laser etching step to allow contact to be made with the surface layer of the cell from the rear of the substrate.

Embodiments of the invention may also employ grooving of the rear surface of the substrate to form thin strong cell structures which have high efficiency and are radiation resistant.

According to a second aspect, the present invention consists in a solar cell comprising a substrate, one surface of which has a plurality of grooves or hollows formed therein, and a rectifying junction formed on said surface and extending into said grooves, a top layer of said junction having a sheet resistivity which is greater in the region between the grooves than in the region within the grooves.

According to a third aspect, the present invention consists in a solar cell comprising a substrate, opposite surfaces of which each have a plurality of grooves or hollows formed therein, a rectifying junction being formed on one of said surfaces and extending into the grooves or hollows of that surface.

Embodiments of the invention will now be described, by way of example, with reference to the accompanying drawings wherein:

FIG. 1 schematically illustrates a sectional view of a solar cell manufactured in accordance with a first embodiment of the present invention;

FIG. 2 schematically illustrates the solar cell of FIG. 1 when viewed from the top;

FIG. 3 schematically illustrates a sectional view of a solar cell manufactured in accordance with a second embodiment of the present invention;

FIG. 4 schematically illustrates a sectional view of a fully etched substrate according to an embodiment of the invention;

FIGS. 5*a*–5*c* schematically illustrate (a) a plan view of a laser scribing pattern; (b) a plan view of a fully etched substrate and (c) a perspective view of a fully etched substrate for a fourth embodiment of the invention;

FIGS. 6*a*–6*c* schematically illustrate (a) a plan view of a laser scribing pattern; (b) a plan view of a fully etched substrate and (c) a perspective view of a fully etched substrate for a fifth embodiment of the present invention;

FIGS. 7*a*–7*b*, 8*a*–8*b*, *and* 9*a*–9*b* schematically illustrate (a) a plan view of a laser scribing pattern and (b) a perspective view of a fully etched substrate for sixth, seventh, and eighth embodiments respectively, of the present invention; and

FIG. 10 schematically illustrates an improved method of connecting electrodes to the embodiment of FIG. 8.

Referring to FIG. 1, a substrate 10 is provided with a back contact 11 and a rectifying junction 12 on opposite surfaces, the junction being formed between the substrate 10, which may be of either p-type or n-type semiconductor material, but in this embodiment is p-type material, and a top layer 13 extending over the top surface of the substrate and which is formed of a semiconductor material of opposite impurity type to the substrate 10. Grooves 14 scribed in the top surface of the substrate by a laser scriber, prior to formation of the junction 12, greatly increase the junction area and at the same time facilitate the collection of minority carriers 15 generated deep within the bulk of the substrate, by placing sections of the junction in closer proximity to the region in which these carriers are generated.

Grooves 14 in the cell surface also improve the anti-reflection properties of the cell by acting as light traps. Light 16*a* striking the surfaces of the cell between the grooves, and which is not absorbed by the cell, will be reflected by the surface and wasted, however, light 16*b* striking a surface of one of the grooves 14, and which is not absorbed, will generally be reflected onto another surface of the groove, depending upon the angle of incidence of the light and the shape of the grooves. For light 16*b* falling normal to the top surface of the cell, the number of reflections within the groove 14 will be large, thereby reducing the percentage of light which is reflected out of the grooves.

A further improvement in the anti-reflective properties of the cell may be achieved by filling the grooves with a transparent material such as silicon oxide, and the slope of the groove walls can be optimized after scribing by an unmasked etch of the entire substrate surface.

As well as the improvement in current density due to the physical positioning of the junction within the groove and the increased area of the junction, a further improvement can be attributed to the production of gettering sites during the laser scribing of the surface of the substrate, thereby allowing an increased degree of gettering during subsequent high temperature processing.

Gettering is the process by which impurities are attracted to certain areas of the substrate during high temperature processing, and typical gettering sites are regions of stress causd by diffusion processes and areas of crystal structure damage as caused by laser scribing. The laser scribing process, being a particularly robust process, creates a significant amount of damage to the crystal structure and accordingly a large number of gettering sites will be produced by this process.

The reduction in the number of impurities in the bulk of the substrate, as a result of gettering, has the effect of increasing the minority carrier life time and accordingly increasing the probability of a minority carrier being collected at the rectifying junction 12 before recombination occurs.

The series resistance of the grooved solar cell can also be decreased by selecting a lower sheet resistivity for the portion of the top layer 13 formed in the grooves 14 than for that used in the portion of the top layer between the grooves. In a non-grooved solar cell, manufactured for terrestrial use, the metal contact grid applied to the top layer is often applied by screen printing in order to keep cost to a minimum, however, screen printing imposes restrictions upon the minimum dimensions achievable, these being a minimum contact width of typically 150 μm and a minimum spacing of at least 3 mm. With these contact dimensions, it is necessary to provide a top layer sheet resistivity in the order of 25Ω/□ to 50Ω/□ to minimize lateral resistance; however, such low values of sheet resistivity degrade the photovoltaic properties of the cell. This problem is less pronounced in cells produced for use in space, as in these cells a more sophisticated method of contact formation is used which allows the use of thinner contacts having a closer spacing, such that higher sheet resistivities can be used without degrading the series resistance of the cell. However, the method of contact formation used in space cells adds considerably to their manufacturing costs.

In the case of grooved cells made according to the present invention, sheet resistivities in the order of 25Ω/□ to 50Ω/□ can be provided for that portion of the top layer 13 within the grooves 14, while sheet resistivities in the order of 100–200Ω/□ can be achieved in the top layer portions between the grooves. Typically the groove would be in the order of 50 μm wide and the space between the grooves would be 100 μm, the metal contact fingers 17 (see FIG. 2) running in the direction normal to the grooves and having the dimensions previously stated for screen printed contacts.

A lower sheet resistivity can be achieved in the grooved regions in numerous ways, some examples of which are:

(a) By using a thickness dependent spin diffusion source, or alternatively a spray-on diffusion source which upon application will automatically give a thicker layer in the groove.

(b) By providing a heavy diffusion over the entire surface, which is followed by a chemical or plasma etch of the exposed regions to increase sheet resistivity.

(c) By using a laser to locally heat the silicon subsequent to the application of a diffusion source.

The low sheet resistivity of the top layer in the grooved regions will have a detrimental effect on the response of the cell to short wavelength (blue) light due to the increased top layer thickness and therefore the sheet resistivity chosen will be a compromise between a value which gives low series resistance and a value which does not seriously degrade the response to blue light. It will be recognised, however, that while low sheet resistivity will degrade the response to blue light, the beneficial effects of low series resistance and improved current density due to increased junction area and the provision of a portion of the junction deep within the bulk of the substrate, will more than make up for this degradation. Further, the low sheet resistivity in the grooves will not seriously affect the response of the cell to long wavelength (red) light.

The use of a low sheet resistivity top layer in the grooved regions of space cells will also allow the contact fingers in these cells to be spaced more widely,

thereby, allowing the use of less costly formation process and accordingly reducing the manufacturing costs of the cell.

Referring now to FIG. 3, the metal contact fingers 17 in FIG. 2 may be replaced by Conductor-Insulator-Silicon (CIS) contacts wherein the top layer 13 is a lightly doped region, the rectifying effect of the junction 12 being reinforced by the MIS contact comprising a thin layer of insulation 18 over the top layer and a metal, or a highly doped polycrystalline, contact finger 19 formed over the insulation layer 18. The fingers 19 will be arranged in a similar configuration to the metal fingers 17 shown in FIG. 2, however, the insulation layer may either be formed over the entire surface of the cell, by using a transparent insulation layer such as a silicon oxide, or alternatively the insulation layer may be only formed in the region of the conductor finger 19.

Referring to FIG. 4 of the drawings, reflection properties of the laser groove cell can be optimised by arranging the grooving so that the sloping groove walls intersect with one another, thereby substantially eliminating the flat intergroove regions illustrated in FIGS. 1, 2, and 3. With the structure of FIG. 4, the only ungrooved regions required are flat paths 21 (refer to FIGS. 5*b* and 5*c*) provided for the top contact metallisation.

As illustrated in FIG. 4, very precise control of such structures can be obtained in single crystal material by using chemical etches with anisotropic properties, combined with laser grooving. For example, dilute caustic soda solutions etch silicon very slowly in the [111] crystal direction but etch very rapidly in other directions. Therefore, if the surface 22 of a wafer has [100] orientation and is grooved by a laser to form grooves 23 and then subsequently etched in dilute caustic soda solutions, the silicon is very quickly etched away until the [111] crystal planes are exposed to form the grooved surface 24 of FIG. 4. Once the [111] crystal planes, coinciding with the faces of the surface 24, are exposed, the rate of etching slows markedly, allowing precise control of the final etched surface shape, thereby allowing the resulting surface geometry of the device to be precisely defined by the depth and spacing of the original grooves 23.

Regardless of the method used to control the slope of the groove walls, interesting and useful structures can be obtained by the use of intermittent grooving of the cell surface and several such structures will now be described with reference to FIGS. 5, 6, 7, 8, and 9.

Referring to FIG. 5, a "slat" structure is illustrated wherein the laser grooving 23 is intermittently broken by gaps 25 in order to provide strengthening ribs or struts 26 in the final etched substrate of FIG. 5(*c*). In addition, a larger gap 27 in the laser grooving pattern results in the flat path 21 in the final etched substrate which provides a location for top contact metallization in the completed cell.

Turning to FIG. 6, the laser grooves 23 of FIG. 5 are replaced by holes 33 which are bored by the laser scriber in the square pattern illustrated in FIG. 6*a*, such that after etching, an inverted pyramid structure as illustrated in FIG. 6*b* and FIG. 6*c* is produced with the top surface 34 of the inverted pyramid structure again corresponding to the [111] crystal planes of the substrate.

Combined grooving of the front and rear surfaces of the wafer and subsequent etching gives rise to a further class of cells which have been termed "crinkle cut" cells. Referring to FIG. 7, if a grooving pattern 43, similar to the pattern 23 of FIG. 5*a* is provided in a top surface of the wafer and a second grooving pattern 53, again similar to the pattern 23 of FIG. 5*a*, is provided in the bottom surface of the wafer and the wafer is subsequently etched, a structure of the form illustrated in FIG. 7*b* will be produced, wherein parallel grooves run along both sides of the wafer, the grooves in one side corresponding with the peaks in the other side of the wafer to provide a corrugated structure having strengthening struts or ribs 46 (underside ribs not shown) and the surfaces 44 and 54 each corresponding to [111] crystal planes of the substrate.

FIGS. 8 and 9 illustrate additional "crinkle cut" structures, the structure of FIG. 8 comprising inverted pyramids similar to those of FIG. 6 on each side of the wafer, with the pyramids on one side of the wafer being offset from those on the other side, while the structure of FIG. 9 has inverted pyramids on the top surface and a crossed groove structure on the bottom surface to provide an etched wafer structure having a substantially constant thickness as is the case with the structure of FIG. 7. The structures of FIG. 7 and FIG. 9 allow very thin strong cells having good reflection properties to be fabricated and these structures will assist in the production of very high efficiency cells with good radiation resistance. The structure of FIG. 8 on the other hand will produce cells having good reflection properties with moderate thickness but great strength.

The laser grooving technique can also be used to produce structures which have holes extending right through the cell from one side to the other. The structures illustrated in FIGS. 6, 8, and 9 are particularly suited to this technique. The advantage of a structure which employs holes passing completely through the cell is that it is then possible to have both contacts to the cell made on the rear surface of the cell, thereby avoiding the losses associated with top contact shading. For example, a section of a structure similar to that of FIG. 6 is illustrated in FIG. 10, wherein the grooving is much greater than that previously illustrated such that the apex 35 of inverted pyramids extends to the back surface of the wafer. With this structure, once the top layer 13 has been formed, metallised top contacts 36 can be provided from the back of the cell at each apex point. This technique allows an improvement in overall cell efficiency by removing the problem of top contract shading which would otherwise occur, while at the same time allowing connections to the top contacts to be of greater current carrying capacity, as the trade off between current carrying capacity and degree of shading is no longer necessary.

The laser used to produce any of the previous laser groove structures can be programmed very simply to punch holes through the cell in any prescribed location so that a variety of such punch through structures are possible with this approach and clearly the punch through technique can be used with any of the structures previously described.

A preferred method of manufacturing laser groove cells requires starting with a silcon wafer of desired surface orientation (for example [100]) and then grooving one or both sides of the cell in the desired pattern using a laser. The wafer is then etched in an appropriate chemical solution to define the shape of the walls of the groove. Thereafter, cell processing proceeds as it would with prior art devices. The top junction is formed by the diffusion of an appropriate dopant and, if desired, a

back surface field region is formed at the rear of the cell. Top and rear contact metallization can then be formed by any chosen sequence, e.g. vacuum deposition, screen printing, or electroplating, as can the antireflection coating.

It will be recognised by persons skilled in the art that numerous variations and modifications may be made to the invention as described above without departing from the spirit or scope of the invention as broadly described.

We claim:

1. A solar cell comprising a substrate, a front surface of which has a plurality of grooves or hollows formed therein, and a rectifying junction formed on said surface and extending into said grooves, a top layer of said junction having a sheet resistivity which is greater in the region between the grooves than in the region within the grooves.

2. A solar cell as claimed in claim 1, wherein the sheet resistivity of the top layer within the grooves is in the order of 25–50Ω/□ while sheet resistivity of the top layer between the grooves is in the order of 100–200Ω/□.

3. A solar cell of claim 2, wherein said grooves comprise through holes provided in said substrate, the lower resistivity regions of the top layer extending into the through holes and along a portion of the rear surface of the cell, metallized contacts to said lower resistivity regions being provided on said rear surface of the substrate to make low resistance electrical contact with the top layer of the junction.

4. A solar cell of claim 1, wherein said grooves comprise through holes provided in said substrate, the lower resistivity regions of the top layer extending into the through holes and along a portion of the rear surface of the cell, metallized contacts to said lower resistivity regions being provided on said rear surface of the substrate to make low resistance electrical contact with the top layer of the junction.

5. A method of manufacturing solar cells, said method comprising the steps of scribing a pattern of grooves or holes in the front surface of a semiconductor substrate with a laser scriber, subsequently etching said grooves or holes with a chemical etchant, said etchant being selected to etch the base region of said grooves or holes more slowly than the top region to convert said grooves to V-shaped troughs and to convert said holes to shapes approximating inverted pyramids, and subsequently forming a rectifying junction on said surface, said junction extending into said troughs or inverted pyramids.

6. The method of claim 5, wherein said laser scriber is used to bore holes through said substrate during the laser scribing step and the junction extends through said holes to cover a portion of the rear surface thereof such that contact can be made with the top layer of the cell from the rear of said substrate.

7. The method of claim 5, wherein grooves or holes are also laser scribed into the rear surface of said substrate prior to the chemical etching step, these grooves or holes being interposed between the grooves or holes formed in the top surface such that, after the chemical etching step, a structure of small average thickness, high strength, and low surface reflectance results.

* * * * *

United States Patent [19]

Nelson

[11] **Patent Number: 4,984,358**

[45] **Date of Patent: Jan. 15, 1991**

[54] **METHOD OF ASSEMBLING STACKS OF INTEGRATED CIRCUIT DIES**

[75] Inventor: **Bradley H. Nelson**, Austin, Tex.

[73] Assignee: **Microelectronics and Computer Technology Corporation**, Austin, Tex.

[21] Appl. No.: **539,769**

[22] Filed: **Jun. 18, 1990**

Related U.S. Application Data

[63] Continuation-in-part of Ser. No. 429,293, Oct. 27, 1989, which is a continuation of Ser. No. 321,500, Mar. 10, 1989, Pat. No. 4,930,216.

[51] **Int. Cl.**[5] **H05K 3/36**

[52] **U.S. Cl.** **29/830**; 29/854; 29/885; 29/412; 29/413; 29/414; 437/226

[58] **Field of Search** 29/830, 854, 855, 885, 29/412–415; 437/226, 227

[56] **References Cited**

U.S. PATENT DOCUMENTS

3,280,019	10/1966	Harding et al.	204/181
3,588,852	6/1971	McCormack et al.	29/830
3,835,531	9/1974	Luttmer	29/830
4,486,738	12/1984	Sadlo et al.	338/320
4,542,397	9/1985	Biegelsen et al.	357/92
4,640,721	2/1987	Uehara et al.	148/188
4,897,918	2/1990	Osaka et al.	29/830

FOREIGN PATENT DOCUMENTS

245099	4/1987	German Democratic Rep.	29/830

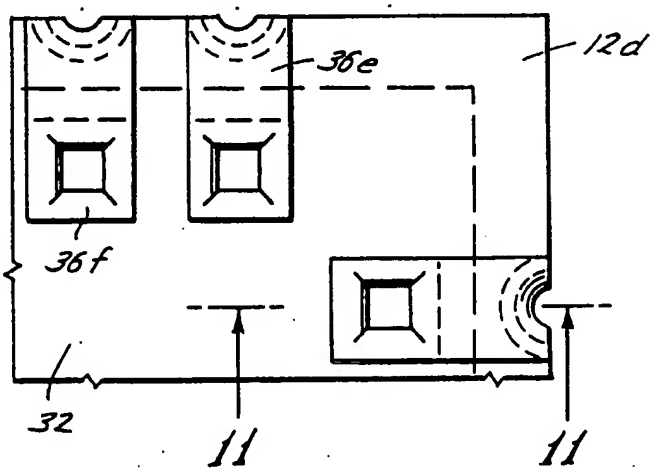
Primary Examiner—P. W. Echols

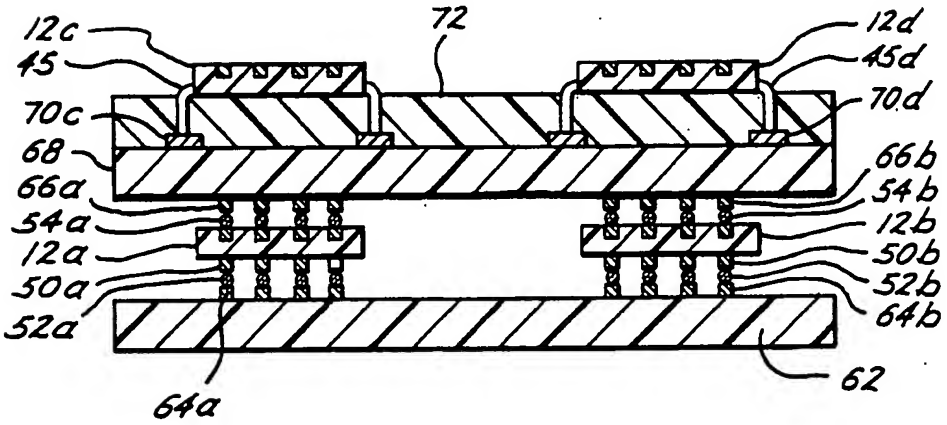
Attorney, Agent, or Firm—David M. Sigmond

[57] **ABSTRACT**

Integrated circuit dies, while still in wafer form, are prepared for stacking without requiring packaging. Holes are made through a wafer having a plurality of integrated circuit dies and are placed between the dies and adjacent the die pads. A layer of insulating material is placed on the wafer and in the outer periphery of the holes. An electrically conductive connection is made between the top of each pad and the inside of the insulating material in an adjacent hole. The insulating layer and the electrically conductive layer can be further extended to the backside of the dies if desired. The dies are separated from each other and can be assembled in a stack and/or surface mounted to a substrate.

20 Claims, 5 Drawing Sheets





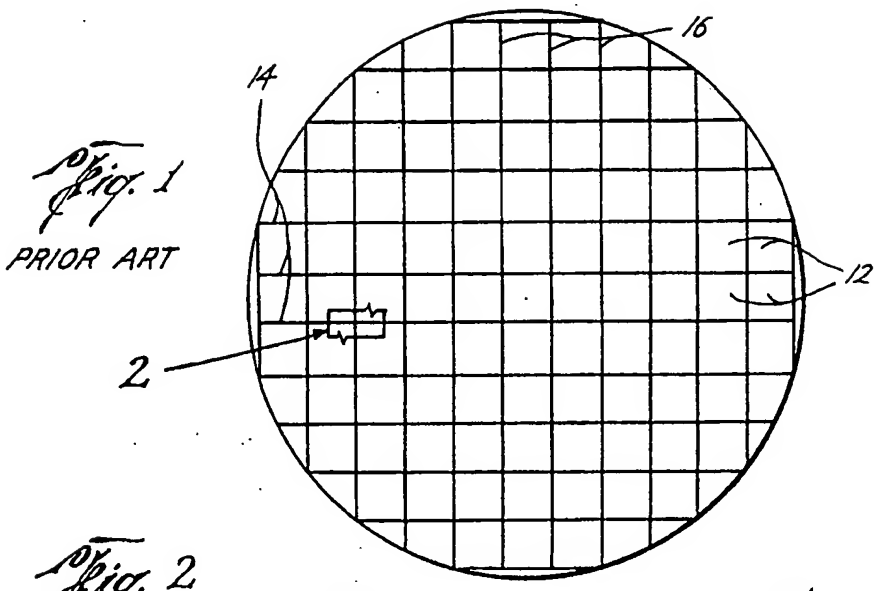


Fig. 1
PRIOR ART

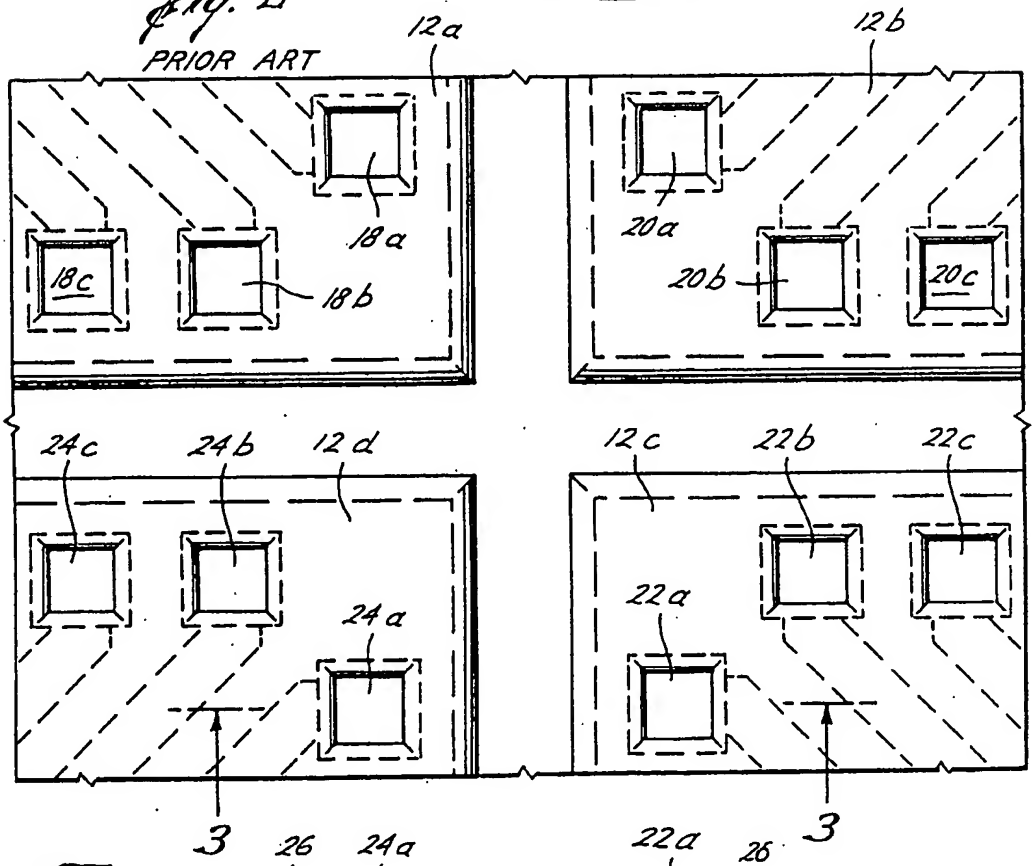


Fig. 2
PRIOR ART

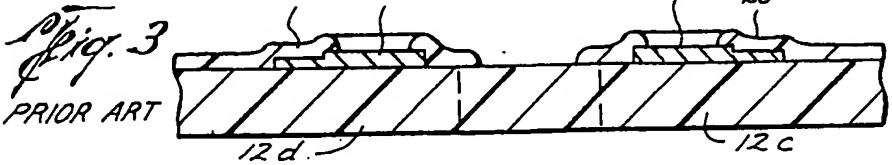


Fig. 3
PRIOR ART

Fig. 4

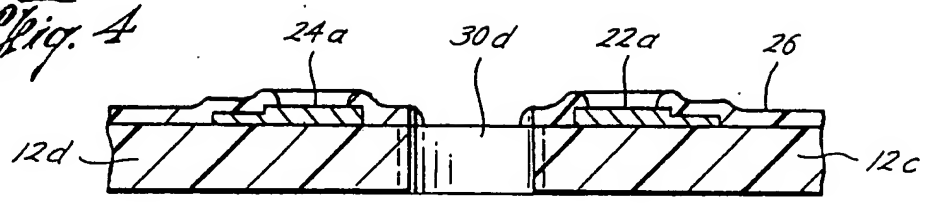


Fig. 5

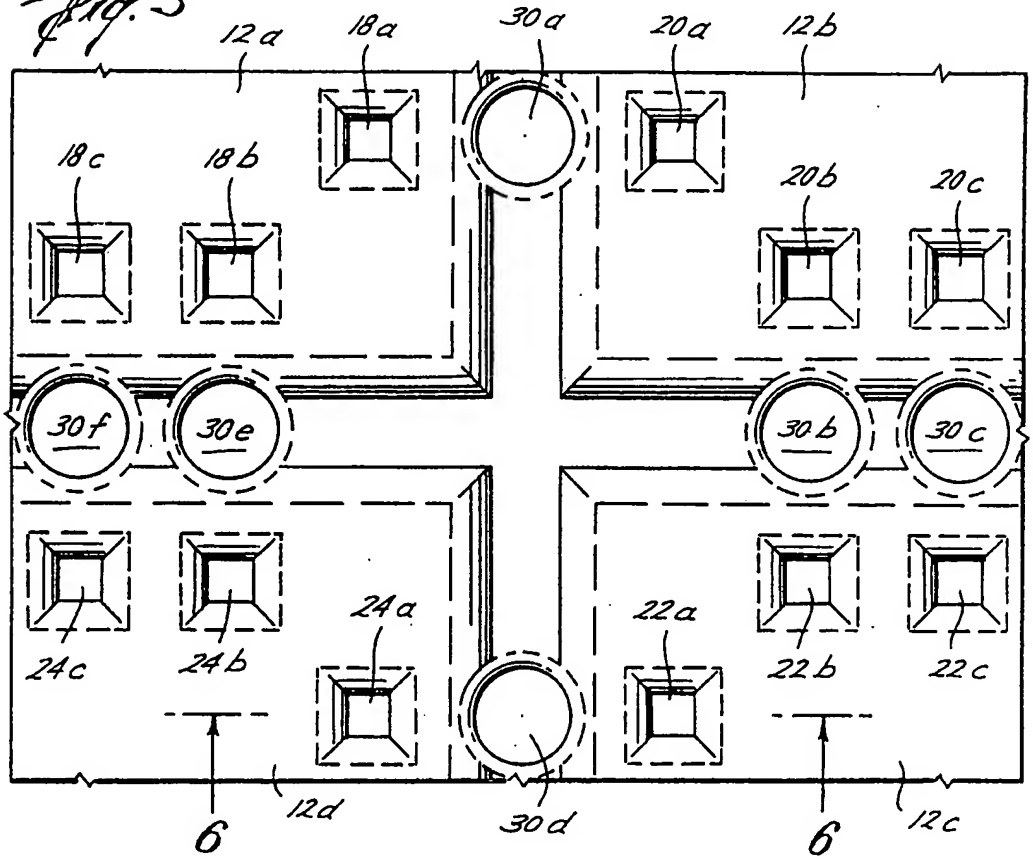


Fig. 6A

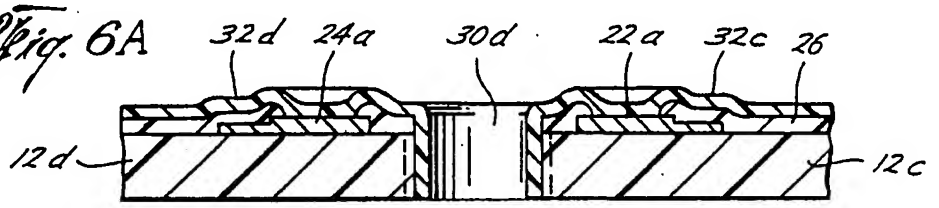


Fig. 7A

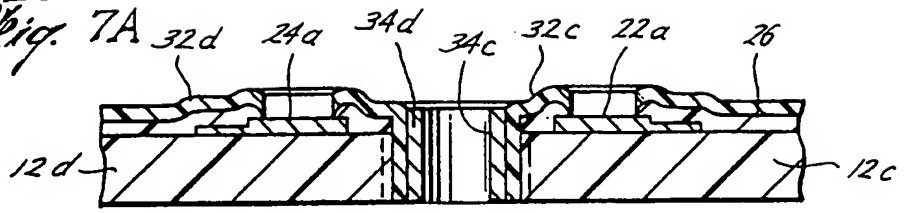


Fig. 8A

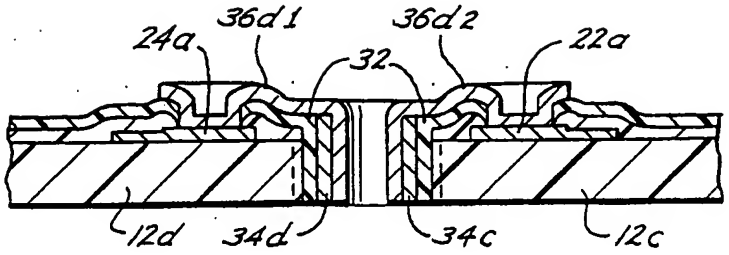


Fig. 6B

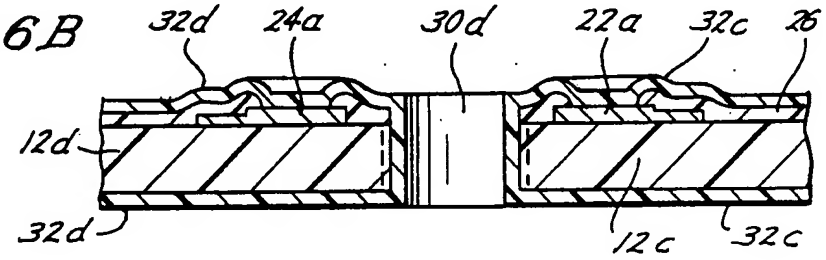


Fig. 7B

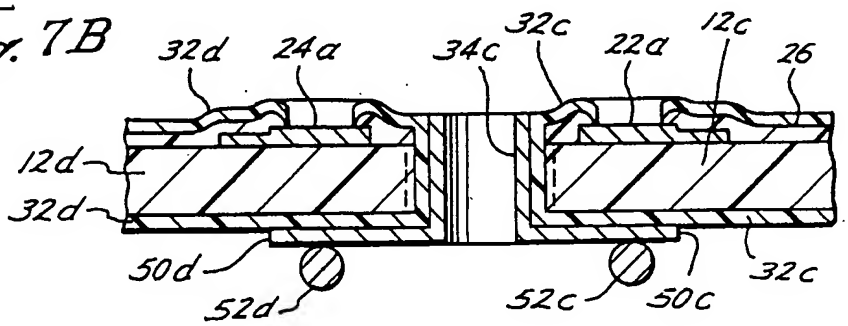


Fig. 8B

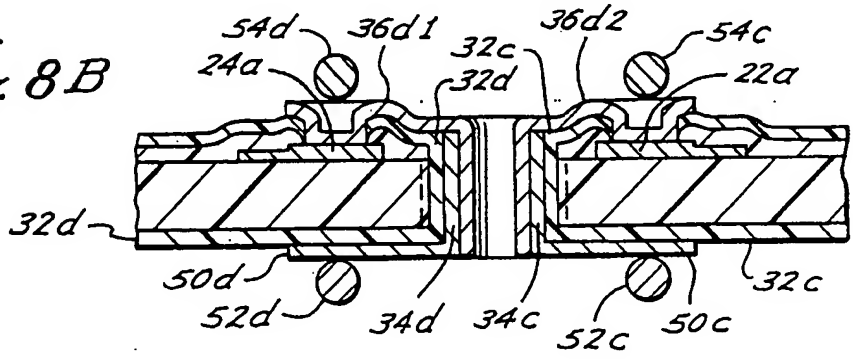


Fig. 9

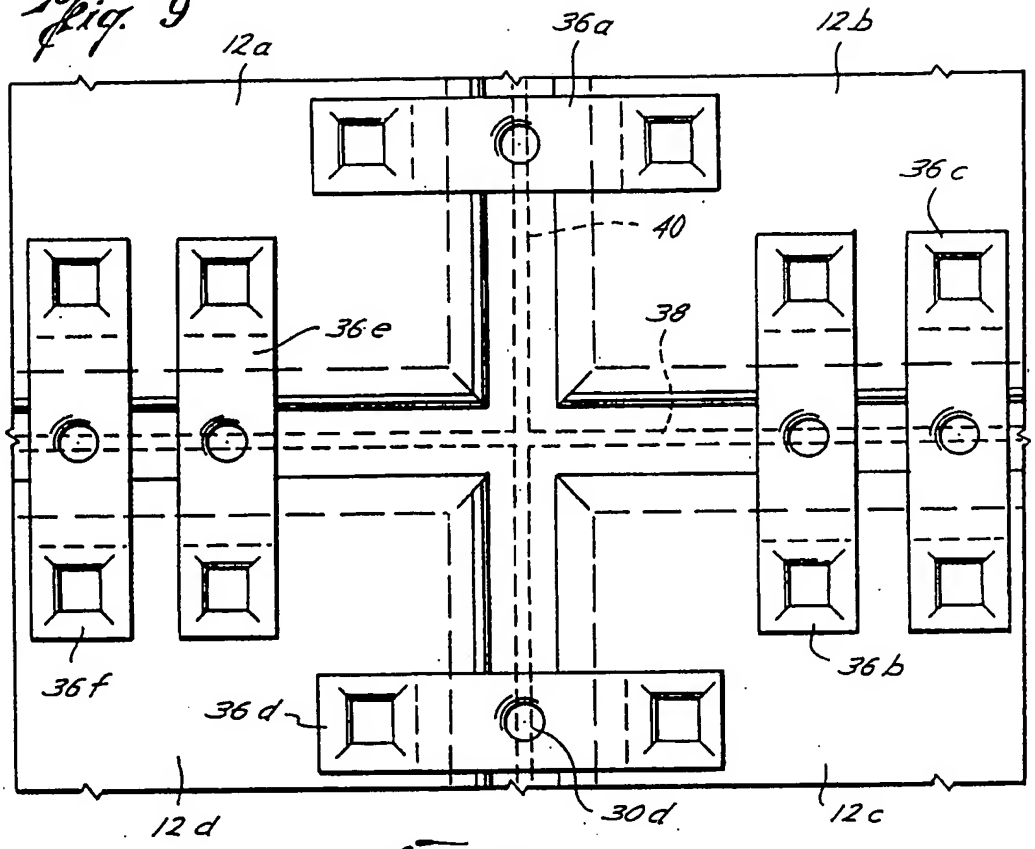


Fig. 10

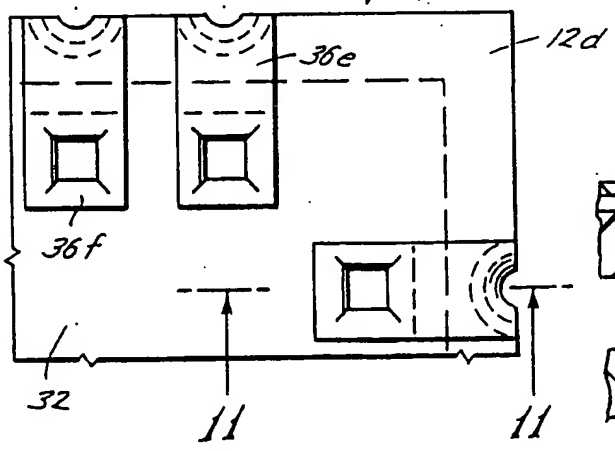
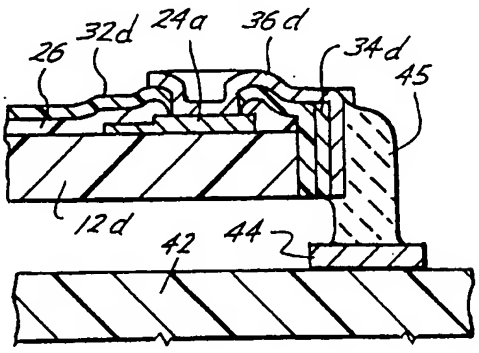


Fig. 11



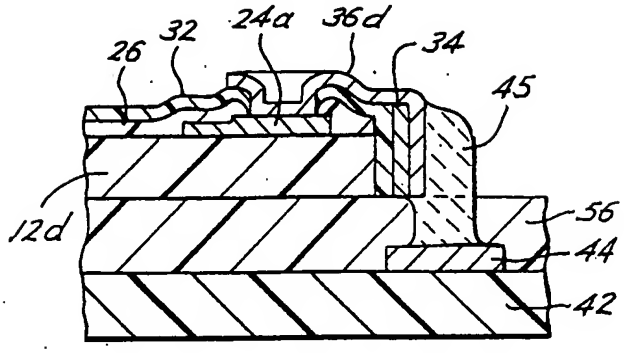


Fig. 12

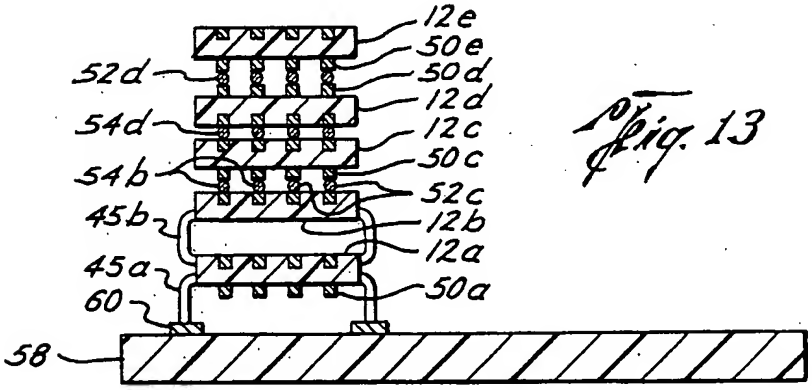


Fig. 13

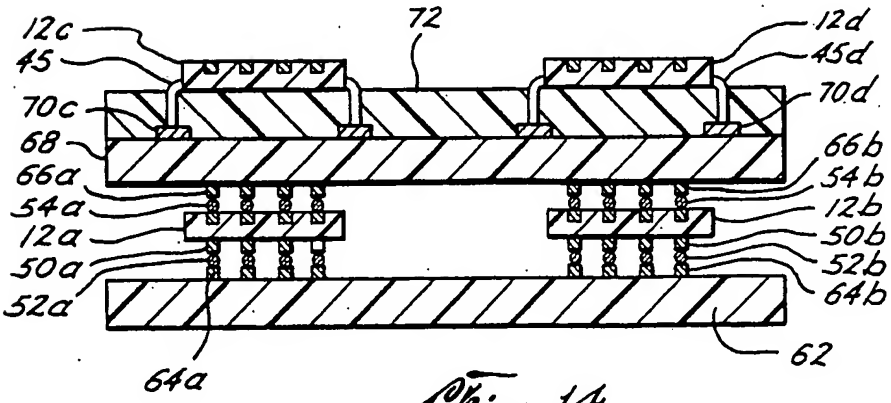


Fig. 14

METHOD OF ASSEMBLING STACKS OF INTEGRATED CIRCUIT DIES

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is a continuation-in-part of U.S. Ser. No. 07/429,293, filed Oct. 27, 1989, entitled "Process For Preparing Integrated Circuit Dies For Mounting," now pending, which is a continuation of U.S. Ser. No. 07/321,500, filed Mar. 10, 1989, entitled "Process For Preparing Integrated Circuit Dies For Mounting," now U.S. Pat. No. 4,930,216.

BACKGROUND OF THE INVENTION

It is known to place an integrated circuit die in a leadless ceramic package having serrated edges on the edges of the package and then solder the package to a substrate.

However, the manufacturing of packaging integrated circuits increases the complexity and expense. The present invention is directed to a method for preparing integrated circuit dies, while still in wafer form, for stacking as well as surface mounting to a substrate without requiring packaging of the dies, while still fabricating the dies in a manner to be corrosion resistant.

SUMMARY

The present invention is directed to a method of assembling stacks integrated circuit dies for mounting on a substrate, and includes making holes through a wafer having a plurality of integrated circuit dies in which the dies include bonding pads thereon connected to the integrated circuits in the dies. Holes are placed between the dies and adjacent the pads. The method includes placing a layer of insulating material over the wafer and in the outer periphery of the holes. An electrically conductive connection is patterned between the top of each bonding pad and the inside of the insulating material in an adjacent hole. The insulating layer and electrically conductive connection can also be applied beneath the dies to their backsides if desired. Thereafter, the plurality of dies are separated from each other along lines extending through the holes between the dies. This leaves the edge of the die metallized, as well as the backside of the die metallized if desired.

An object of the present invention is interconnection of dies between the electrically conductive connections on the inside of the cut holes.

Yet another object of the present invention is interconnection of the dies between the electrical conductors on the backside of a die and the pads on the top of a separate die.

Another object of the present invention is connecting a die to a substrate by an electrical interconnection to the electrically conductive connection on the inside of the cut holes.

Still another object of the present invention is wherein the holes are placed between pads on adjacent dies whereby each hole may be connected to two pads.

Yet a still further object of the present invention is wherein scribe lines are positioned on the wafer between adjacent dies and the holes are placed on the scribe lines.

A still further object of the present invention is the addition of a protective dielectric layer between a die and an interconnected component.

A further object of the present invention is a method of assembling stacks of integrated circuit dies by making holes through a wafer having a plurality of integrated circuit dies in which the dies include pads thereon connected to integrated circuits in the dies. The holes are placed between the dies and adjacent the pads. A layer of insulating material is placed over the wafer and in the outer periphery of the holes, as well as on the backside beneath the die if desired. The insulating material is then removed from the tops of the pads. An electrically conductive layer is added to the inner periphery of the insulating materials in the holes and an electrical connection is added between the top of each pad and the conductive layer in the holes, and electrical conductors connected to the conductive layer in the holes can be applied to an insulator layer beneath the die if desired. The plurality of dies are separated, such as by sawing, along the lines passing through the holes between the dies. A stack of dies car be connected together, or a die can be connected to a substrate.

Other and further objects, features and advantages will be apparent from the following description of a presently preferred embodiment of the invention, given for the purpose of disclosure, and taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is an elevational view of a conventional wafer having a plurality of integrated circuit dies,

FIG. 2 is an enlarged elevational view of the intersection 2 of FIG. 1,

FIG. 3 is a cross-sectional view taken along the line 3—3 of FIG. 2,

FIG. 4 is a view similar to FIG. 3 with the addition of the steps of providing holes through the wafer between adjacent dies,

FIG. 5 is an elevational view of the structure of FIG. 4 with the addition of an insulating layer over the wafer and on the inside periphery of the holes,

FIGS. 6A and 6B are cross-sectional views taken along the line 6—6 of FIG. 5,

FIGS. 7A and 7B are views similar to FIGS. 6A and 6B showing the step of removing the insulation from the top of the bonding pads on the dies and with the addition of a electrical conductor layer on the inside circumference of the holes,

FIGS. 8A and 8B are views similar to FIGS. 7A and 7B with the addition of an electrical connection between the pads and the conductive layer on the inside circumference of the holes,

FIG. 9 is an elevational view of the structure of FIG. 8 and also indicating cutting lines between adjacent dies along which the dies are separated,

FIG. 10 is a fragmentary elevational view illustrating one of the dies of FIG. 9 which has been separated from the wafer, and

FIG. 11 is a cross-section taken along the line 11—11 of FIG. 10 with the addition of a soldering connection between, the die and a substrate,

FIG. 12 is a cross-section similar to FIG. 11 in which a dielectric layer is added between the die and a substrate,

FIG. 13 is a cross-sectional view of a particular stacking arrangment of dies that can be assembled in accordance with the present invention, and

FIG. 14 is a cross-sectional view similar to FIG. 13 showing another stacking arrangement of dies.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring now to the drawings, the reference numeral 10 generally indicates a conventional wafer, such as a silicon wafer, having a plurality of integrated circuit dies 12 thereon and conventional scribe lines 14 and 16 thereon between adjacent dies 12 along which the wafer 10 is conventionally sawed for separating the dies 12.

Referring now to FIGS. 2 and 3, an enlarged plan view and section view of a portion of the wafer 10 is shown in which the individual dies are numbered 12*a*, 12*b*, 12*c* and 12*d* for convenience. As is conventional, each of the dies includes a plurality of bonding pads which are connected to the integrated circuits for providing for connection of the dies to other components. For example, die 12*a* includes a plurality of bonding pads 18*a*, 18*b*, and 18*c*. Die 12*b* includes a plurality of bonding pads 20*a*, 20*b*, and 20*c*. Die 12*c* includes a plurality of bonding pads 22*a*, 22*b* and 22*c*, and die 12*d* includes a plurality of bonding pads 24*a*, 24*b* and 24*c*. As is conventional, an insulating layer 26 is provided over the dies 12. The bonding pads are generally metallic such as aluminum.

The above description of a wafer 10 and its components is conventional. Normally, the wafer 10 is sawed along the scribe lines 14 and 16 separating the individual integrated circuit dies 12 from each other and they can be encapsulated in a package having serrated edges for soldering the package to a substrate, which is expensive.

The present invention is directed to a method for preparing the integrated circuit dies, while still in wafer form for stacking as well as surface mounting direct to a substrate without requiring an expensive package.

Referring now to FIGS. 4 and 5, a plurality of holes, for example 5 mil diameter holes, are made through the wafer 10 between the dies 12 and adjacent the bonding pads. The holes may be made by any suitable means such as etching, or ultra-sonic drilling. Preferably, the holes are made on the scribe lines 14 and 16, and where possible between adjacent pads on adjacent dies for allowing each hole to be connected to two pads as will be more fully described hereinafter.

Referring now to FIGS. 6A and 6B, hole 30*a* may be made through the wafer 10 between dies 12*a* and 12*b* between pads 18*a* and 20*a*. Hole 30*b* is between dies 12*b* and 12*c* between pads 20*b* and 22*b*, hole 30*c* is between dies 12*b* and 12*c* between pads 20*c* and 22*c*, hole 30*d* is between dies 12*c* and 12*d* between pads 24*a* and 22*a*, hole 30*e* is between dies 12*a* and 12*d* between pads 18*b* and 24*b*, and hole 30*f* is between dies 12*a* and 12*d* between pads 18*c* and 24*c*. A layer of insulating material 32 seen as 32*c* for die 12*c* and 32*d* for die 12*d*, such as silicon oxide or silicon nitride, is applied over the wafer 10 and in the outer periphery of but not filling the holes, such as by the process of chemical vapor deposition. Alternatively, as seen in FIG. 6B, insulating material 32 can also be applied beneath wafer 10 along its backside, in the same step if desired. A preferred thickness of insulating material 32 is 1–2 microns.

Hermetic sealing considerations often play an important role in wafer manufacturing. In accordance with the present invention, silicon nitride will provide a better hermetically sealing insulator 32 than silicon oxide. However, a still better hermetic seal by insulator 32 is acheived by first applying a layer of silicon oxide, for instance 0.5 micron, and then applying a layer of silicon nitride, for instance 0.5 micron. While the two separate layers each tend to form pinholes, the pinholes form in different locations, and the likelihood of aligning pinholes is small. Thus the pinholes are likely to be plugged. A tight hermetic seal can also be formed by covering insulator material 32, preferably silicon nitride, with an organic dielectric such as Parylene. Parylene is a conformal polymer coating which uniformly protects various configurations of parts, such as sharp edges and points. Parylene is the generic name for members of a unique polymer series developed by Union Carbide Corporation. A parylene coating of 0.1 to 76 microns can be applied in a single operation.

As best seen in FIGS. 7A and 7B, the insulating material 32 is removed from the top of the bonding pads such as by patterning with photoresist and reactive ion etching or wet chemical etching. If insulating layer 32 comprises different materials, such as silicon oxide and silicon nitride, then different etchants may be required. However, silicon oxide and silicon nitride can be removed in a single dry plasma etch despite their different etch rates. As an alternative, the insulating layer 32 may be placed over the wafer 10 in the step of FIGS. 6A and 6B leaving the top of the pads bare, but it is preferable to use the step shown in FIGS. 6A and 6B of coating the entire wafer with the insulating layer 32 and then removing it from the pads, as shown in FIGS. 7A and 7B, for ease of manufacture. After the inside of the holes have been insulated an electrically conductive layer 34, such as copper, gold, or aluminum, shown as 34*c* and 34*d* for dies 12*c* and 12*d* respectively, is placed around the inner periphery of but not filling the insulating material 32 in the holes, for instance by pattern electroplating. preferred thickness of electrically conductive layer 34 is 1–10 microns.

Referring further to FIG. 7B, if desired, backside electrical conductors 50, shown as 50*c* and 50*d* for dies 12*c* and 12*d* respectively, can be applied to the bottom of insulating layer 32 in a separate step. It is necessary to apply insulating layer 32 between wafer 10 and conductors 50 in order to prevent conductors 50 from short-circuiting wafer 10. Conductors 50 are electrically connected to electrically conductive layer 34, so pads 22*a* and 24*a* can be electrically interconnected to conductors 50*c* and 50*d*, respectively, beneath wafer 10. Conductors 50 can be patterned by numerous methods known to those having skill in the art, such as electroplating, electroless plating, laser direct write, or chemical vapor deposition. A suitable pattern, for instance, would be an array with conductors 50 properly spaced for alignment with a die and/or substrate to be mounted on. A preferred thickness of backside conductors 50 is 1–10 microns. To facilitate interconnection to another die or substrate, bumps 52, shown as 52*c* and 52*d*, can be deposited on conductors 50*c* and 50*d* respectively. Bumps 52 can, for example, be formed of solder, gold, tin-lead alloys, or electrically conductive adhesives. Solder and tin-lead alloys would be advantageous in reflowable bonding operations. A preferred size for bumps 52 is 0.5–2.0 mils. There are several well known methods for patterning bumps on conductors; see, for example, P. A. Totta and R. P. Sopher, "SLT Device Metallurgy and its Monolighic Extension," *IBM Journal of Research Developement*, pp. 226-238 (1968); K. Hatada, H. Fujimoto and K. Matsunaga, "New Film Carrier Assembly Technology: Transferred Bumps TAB," *IEEE Transactions on Components, Hybrids, and Manufacturing Technology*, Vol. CHMT-10, No. 3

(1987); and U.S. Pat. No. 3,303,393 entitled "Terminals For Microminiaturized Devices and Methods of Connecting Same to Circuit Panels," which issued in Feb. 1967. In any event, it is understood that the presence of bumps is not essential to dies manufactured in accordance with the present invention, since the bumps or other means of electrical interconnection can instead be attached to the component that the die will be interconnected and stacked. In another embodiment, backside conductors **50** can be applied after electrically conductive connections **36***a*-**36***f* are added, as long as backside conductors **50** are electrically connected to conductors **34**, **36**, or both.

Referring now to FIGS. **8**A, **8**B and **9**, an electrically conductive connection **36***a*, **36***b*, **36***c*, **36***d*, **36***e*, and **36***f* is added between the top of each pad, such as copper, gold, or aluminum, by a process such as pattern electroplating or sputter deposition followed by resist patterning and wet etch, to the layer **34** in an adjacent hole. If desired, the step of FIGS. **7**A and **7**B of adding the layer **34** may be omitted and combined with the step of FIGS. **8**A and **8**B of adding the electrical interconnection between the interior of the hole and the pad. Electrical conductive connection **36***d* is shown as connection **36***d***1** connecting pad **24***a* to conductor **34***d* in hole **30***d* as well as backside conductor **50***d*, if any. Likewise, connection **36***d***2** connects pad **22***a* to conductor **34***c* in hole **30***d* as well as backside conductor **50***c*, if any. Similarly, the other electrically conductive connections **36***a*, **36***b*, **36***c*, **36***e*, and **36***f* join preferably two pads to the interior of a single hole, as well as any backside conductors **50**. In yet another embodiment, if desired, bumps **54** shown as **54***c* and **54***d* can be deposited on pads **22***a* and **24***a* respectively, with or without the presence of bumps **52**.

As best seen in FIG. **9**, cut lines **38** and **40** are illustrated in dotted outline coaxially along the scribe lines **14** and **16** (not numbered). A normal separation operation, such as conventional sawing, is used for separating the individual dies **12** in the wafer **10**. It is to be noted that the separation occurs along lines **38** and **40** which extend through the holes between the dies. The result of separating the dies from each other is shown in FIG. **10** in which each of the dies is covered with an insulating layer **32** and having an electrical conductive connection from each of the pads extending to the edge of the die into the holes which have been cut and are provided with an electrical connection on the inside of the cut hole and any backside conductors **50**.

As best seen in FIG. **11**, a die such as die **12***d* may now be connected to any suitable substrate such as a silicon substrate **42**, having a pad **44** which is connected to one of the connections on the die **12***d* by soldering **45** between the pad **44** and the electrical connection **36***d*.

Referring now to FIG. **12**, though not essential to the present invention, preferably a dielectric layer **56** is placed between die **12***d* and substrate **42**. Dielectric **56** can provide mechanical as well as corrosive protection to the underlying metallization. A preferred dielectric is polyimide, however teflon is also suitable. A polyimide coating **56** can be applied after die **12***d* and substrate **42** are soldered together. Alternatively, polyimide **56** can be placed over die **12***d* or substrate **42** and then selectively laser drilled to open holes where electrical interconnection is required.

The present invention thereby provides an inexpensive integrated circuit which can be easily surface mounted directly to a substrate and which could also be extended for assembling stacks or 3-D arrays of devices as well as providing an integrated circuit that is very reliable in terms of corrosion resistance.

FIGS. **13** and **14** show, for illustration purposes only, various stacking arrangements of dies that can be assembled in accordance with the present invention. FIG. **13** shows die **12***a* mounted to a substrate **58** by connections **45***a* between the inside of the cut holes on die **12***a* and pads **60** on substrate **58**, die **12***b* stacked on die **12***a* by connections **45***b* between the inside of cut holes of dies **12***a* and **12***b*, die **12***c* stacked on die **12***b* by bump connections **54***b* and **52***c* between the pads on die **12***b* and the backside conductors **50***c* on die **12***c*, die **12***d* flipped over and stacked on die **12***c* by bump connections **54***d* between the pads on die **12***c* and the pads on die **12***d*, and die **12***e* stacked on die **12***d* by interconnecting backside conductors **50***e* and **50***d* with bumps **52***d*. It is understood that the bumps between dies **12***b* and **12***c* could initially be attached to the lower die **12***b*, such as bumps **54***b*, or the upper die **12***c*, such as bumps **52***c*. Also, dies that will not have backside interconnections such as die **12***a* may or may not include backside conductors **50***a*. Likewise, FIG. **14** showns dies **12***a* and **12***b* connected to a first substrate **62** by connection bumps **52***a* and **52***b* between substrate pads **64***a* and **64***b* and backside conductors **50***a* and **50***b* respectively. Dies **12***a* and **12***b* are further connected to pads **66***a* and **66***b* on a second substrate **68** by bumps **54***a* and **54***b* respectively. Dies **12***c* and **12***d* are connected to pads **70***c* and **70***d* on the opposite side of substrate **68** by electrical interconnections **45***c* and **45***d* extending to the conductors on the inside of their respective cut holes, wherein the conductors are electrically connected to pads on dies **12***c* and **12***d* as previously described. Additionally, polyimide layer **72** can be coated between substrate **68** and dies **12***c* and **12***d*.

The present invention, therefore, is well adapted to carry out the objects and attain the ends and advantages mentioned as well as others inherent therein. While a presently preferred embodiment of the invention has been given for the purpose of disclosure, numerous changes in the details of construction, arrangement of parts, and steps of the process, will be readily apparent to those skilled in the art and which are encompassed within the spirit of the invention and the scope of the appended claims.

What is claimed is:

1. A method for assembling a stack of integrated circuit dies, comprising:
   - making holes through a wafer having a plurality of integrated circuit dies in which the dies include pads thereon connected to integrated circuits in the dies, said holes being placed between the dies and adjacent the pads;
   - placing a layer of insulating material over the wafer and in the outer periphery of the holes;
   - adding an electrically conductive connection between the top of each pad and the inside of the insulating material in an adjacent hole;
   - separating the plurality of dies from each other along lines extending through the holes between the dies; and
   - connecting a plurality of dies by an electrical interconnection between the electrically conductive connections on the inside of the cut holes of the dies.

2. The method of claim 1 further including connecting a die to a substrate by an electrical interconnection

to the electrically conductive connection on the inside of the cut holes of the die.

3. The method of claim 1 wherein the holes are placed between pads on adjacent dies.

4. The method of claim 1 wherein scribe lines are positioned on the wafer between adjacent dies and the holes are placed on the scribe lines.

5. The method of claim 1 further including adding a dielectric layer between the top of a lower die and the bottom of an adjacent upper die after the dies are electrically interconnected.

6. A method of assembling a stack of integrated circuit dies, comprising:

making holes through a wafer having a plurality of integrated circuit dies in which the dies include pads thereon connected to integrated circuits in the dies, said holes being placed between the dies and adjacent the pads;

placing a layer of insulating material over the wafer and in the outer periphery of the holes;

removing the insulating material from the top of the pads;

adding an electrically conductive connection between the top of each pad and the inside of the insulating material in said adjacent hole;

separating the plurality of dies from each other along lines passing through holes between the dies; and

connecting a plurality of dies by an electrical interconnection between the electrically conductive connections on the inside of the cut holes of the dies.

7. A method for assembling a stack of integrated circuit dies, comprising:

making holes through a wafer having a plurality of integrated circuit dies in which the dies include pads thereon connected to integrated circuits in the dies, said holes being placed between the dies and adjacent the pads;

placing a layer of insulating material over the wafer, in the outer periphery of the holes, and beneath the wafer along its backside;

adding an electrically conductive connection between the top of each pad, the inside of the insulating material in an adjacent hole, and the bottom of the insulating layer beneath the wafer so that the pads are electrically interconnected to conductors beneath the wafer; and

separating the plurality of dies from each other along lines extending through the holes between the dies.

8. The method of claim 7 wherein the holes are placed between pads on adjacent dies.

9. The method of claim 7 wherein scribe lines are positioned on the wafer between adjacent dies and the holes are placed on the scribe lines.

10. The method of claim 7 further including connecting a plurality of dies by an electrical interconnection between the electrically conductive connections on the inside of the cut holes of the dies.

11. The method of claim 7 further including connecting a die to a substrate by an electrical interconnection to the electrically conductive connection on the bottom of the die.

12. The method of claim 7 further including connecting a plurality of dies by an electrical interconnection between the pads on the top of a first die and the conductors on the bottom of a second die.

13. The method of claim 12 further including adding a dielectric layer between the top of a first die and the bottom of an adjacent second die after the dies are electrically interconnected.

14. The method of claim 12 further including connecting electrically conductive bumps to the pads on the top of a die.

15. The method of claim 12 further including connecting electrically conductive bumps to the conductors on the bottom of a die.

16. The method of claim 15 wherein the electrically conductive bumps form an array pattern.

17. The method of claim 15 wherein the electrically conductive bumps are metals selected from the group consisting of solder, gold, and tin-lead alloys.

18. The method of claim 15 wherein the electrically conductive bumps are electrically conductive adhesives.

19. A method of assembling a stack of integrated circuit dies, comprising:

making holes through a wafer having a plurality of integrated circuit dies in which the dies include pads thereon connected to integrated circuits in the dies, said holes being placed between the dies and adjacent the pads;

placing a layer of insulating material over the wafer, in the outer periphery of the holes, and beneath the wafer;

removing the insulating material from the top of the pads;

adding an electrically conductive connection between the top of each pad, the inside of the insulating material in an adjacent hole, and the bottom of the insulating layer beneath the wafer so that the pads are electrically interconnected to conductors beneath the wafer; and

separating the plurality of dies from each other along lines passing through holes between the dies.

20. The method of claim 19 further including connecting a plurality of dies by an electrical interconnection between the pads on the top of a first die and the conductors on the bottom of a second die.

* * * * *

UNITED STATES PATENT OFFICE
CERTIFICATE OF CORRECTION

Patent No. 4,984,358 Dated Jan. 15, 1991

Inventor(s) B. Nelson

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 2, line 19, change "car" to -- can --.

Column 2, line 60, delete "," after "between".

Column 4, line 34, insert -- A -- after "electroplating.".

Signed and Sealed this

Twenty-ninth Day of September, 1992

Attest:

DOUGLAS B. COMER

Attesting Officer

Acting Commissioner of Patents and Trademarks

US005468652A

United States Patent [19]

Gee

[11] Patent Number: 5,468,652

[45] Date of Patent: Nov. 21, 1995

[54] **METHOD OF MAKING A BACK CONTACTED SOLAR CELL**

[75] Inventor: **James M. Gee**, Albuquerque, N.M.

[73] Assignee: **Sandia Corporation**, Albuquerque, N.M.

[21] Appl. No.: **289,161**

[22] Filed: **Aug. 11, 1994**

Related U.S. Application Data

[62] Division of Ser. No. 92,298, Jul. 14, 1993, abandoned.

[51] **Int. Cl.**[6] **H01L 31/18**

[52] **U.S. Cl.** **437/2**; 136/256; 437/180; 437/197; 437/203

[58] **Field of Search** 437/2–5, 180, 437/197, 203–204; 136/256

[56] **References Cited**

U.S. PATENT DOCUMENTS

3,903,427	9/1975	Pack	250/208.2
3,903,428	9/1975	DeJong	136/244
4,227,942	10/1980	Hall	136/255
4,427,839	1/1984	Hall	136/255
4,626,613	12/1986	Wenham et al.	136/255
4,838,952	6/1989	Dill et al.	136/256

FOREIGN PATENT DOCUMENTS

2-51282	2/1990	Japan	136/256

OTHER PUBLICATIONS

J. M. Gee et al, "Emitter Wrap–Through Solar Cell," 23rd IEEE Photovoltaic Specialists Conference, Louisville Ky. (May/1993), pp. 265–270.

T. Warabisako, et al., "A 16.87% Efficient 100 cm^2 Polycrystalline Silicon Solar Cell with Triode Structure," 12–16 Oct. 1992 (Oral Presentation), pp. 172–175, Montreaux, Switzerland.

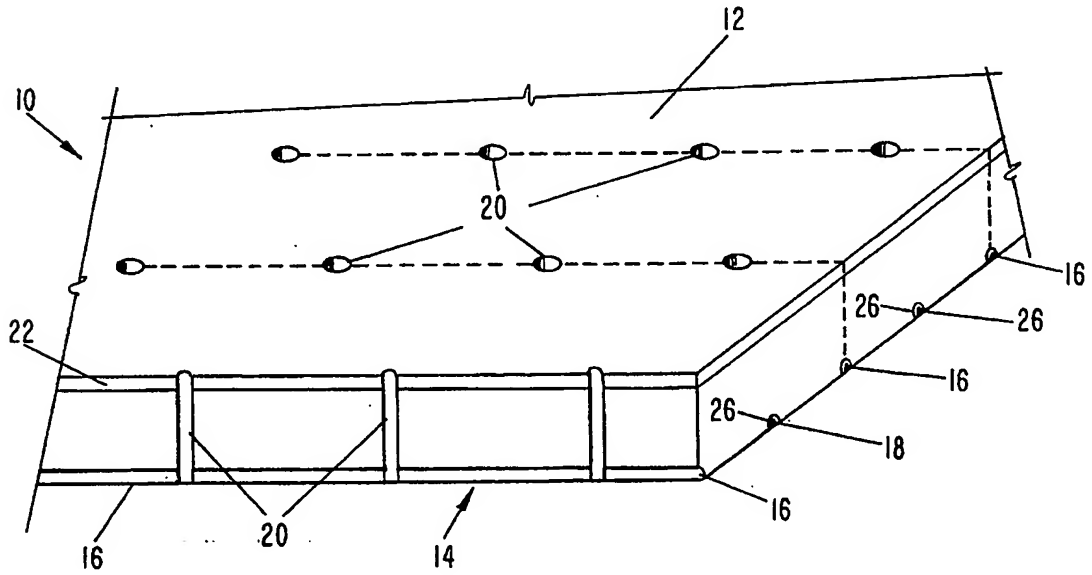
Primary Examiner—Aaron Weisstuch

Attorney, Agent, or Firm—Gregory A. Cone

[57] **ABSTRACT**

A back-contacted solar cell having laser-drilled vias connecting the front-surface carrier-collector junction to an electrode grid on the back surface. The structure may also include a rear surface carrier-collector junction connected to the same grid. The substrate is connected to a second grid which is interdigitated with the first. Both grids are configured for easy series connection with neighboring cells. Several processes are disclosed to produce the cell.

15 Claims, 1 Drawing Sheet



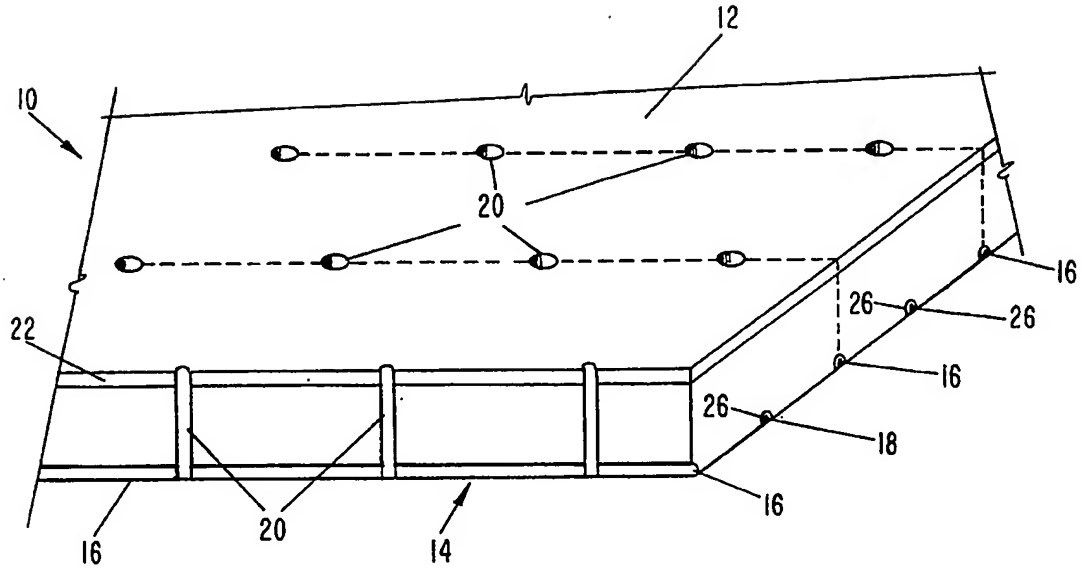


FIG-1

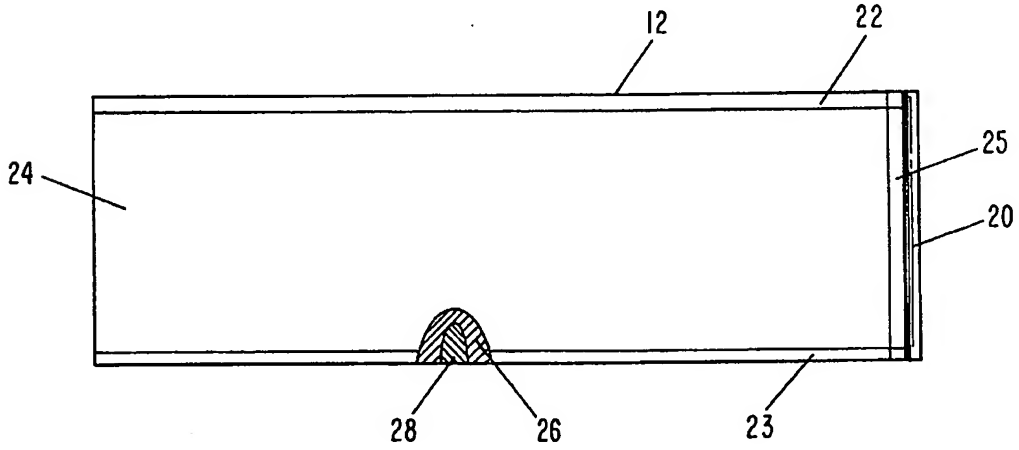


FIG-2

METHOD OF MAKING A BACK CONTACTED SOLAR CELL

BACKGROUND OF THE INVENTION

The government has rights in this invention purs this invention pursuant to Contract No. DE-AC04-76DP00789 awarded by the U.S. Department of Energy. This is a divisional application based on U.S. Ser. No. 08/092,298, filed Jul. 14, 1993, now abandoned.

This invention relates to solar cells (photovoltaic cells) that are back-contacted in that both the negative and positive electrode grids are on the back side of the device. The charges collected in the front-side n-type region are conducted to the back through laser-drilled vias.

Most commercial one-sun solar cells have a carrier-collection junction on the front surface for good collection efficiency. Most commercial one-sun solar cells also have a current-collection grid of one polarity on the front surface and a grid or full-area contact on the back surface of the opposite polarity. Although this is a relatively simple layout and optimizes collection efficiency, the presence of the front grid creates a shadow on the underlying semiconductor junction which adds inefficiency in this respect. Minimizing the shadow loss of the front grid increases the electrical resistance. Other problems associated with this design include increased complexity for cell manufacturing due to the requirement for fine-line grid definition and increased complexity of module assembly due to front-to-back cell stringing and to encapsulation of a non-uniform surface.

Placing both the negative and the positive current-collection grids on the back surface of the solar cell (i.e. "back contact") has several advantages compared to the front-grid cell. Back-contact cells have no grid obscuration losses; the grid design's only constraint is the technological limits of the metallization technology. Grid obscuration and grid resistance losses account for 15 to 20% of the power available in typical commercial one-sun silicon solar cells. Also, module assembly is simplified with back-contact cells since cell stringing does not require front-to-back tabbing and the back-contact cell presents a uniform front surface for encapsulation.

There are two approaches for placing both contacts on the back surface of a solar cell. In the first approach, collection junctions and grids for both polarities are located on the back surface ("back-junction" cell). In this structure, the photogenerated carriers must diffuse to the back surface for collection; hence, these cells require materials with diffusion lengths larger than the device width for good photocarrier collection efficiency. The back-junction cells are therefore not useful with many solar-grade materials that generally have short-diffusion lengths.

The second approach for placing both contacts on the back surface of the solar cell keeps the carrier-collection junction on the front surface, which is more desirable for good collection efficiency in materials with short diffusion lengths. This approach requires vias through the substrate for the current-collection grid on the back surface to contact the carrier-collection junction on the front surface. Two patents have issued to R. H. Hall, U.S. Pat. No. 4,227,942 for "Photovoltaic Semiconductor Devices and Methods of Making Same" and U.S. Pat. No. 4,427,839 for "Faceted Low Absorptance Solar Cell," which disclose solar cells in which both positive and negative grids are arrayed on the back side of the device. The current-collection grid on the back makes

contact to the carrier-collection junction ("emitter") on the front surface through holes in the silicon wafer. These holes are formed by chemical etching. The grids and chemical-etch mask patterns are formed by photolithography. These processes are very expensive and very difficult to use successfully. The cells disclosed by Hall suffer from non optimum contact geometry because of the large areas devoted to the metal grids. This approach has not been pursued commercially.

U.S. Pat. No. 4,626,613 to Stuart R. Wenham and Martin A. Green for "Laser Grooved Solar Cells" discloses solar cells with both contacts on the back surface and with laser-drilled vias for conducting current from the front junction to the appropriate grid on the back surface. This disclosure, however, is in the context of an intricately etched front surface and complex laser-grooving, resulting in an expensive and difficult to produce cell. The cell of the present invention remains as a planar structure without the deep surface etching of the '613 reference and is much easier to produce.

SUMMARY OF THE INVENTION

A very efficient and readily manufacturable solar cell with a front carrier-collection junction can be produced with both negative and positive current-collection grids located on the back side of the device. The invention uses laser-drilled vias to conduct current from the front surface carrier-collection junction to a grid on the back surface. These vias are treated for high conductivity and to electrically isolate the via from the bulk semiconductor. The vias are connected on the back side to one of the current-collection grids. The other (opposite polarity) grid is connected to the bulk semiconductor with doping opposite to that of the collection junction on the front surface. The two grids are interdigitated and optimized to minimize electrical resistance and carrier recombination.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is an isometric cross section of a version of the back-contacted front junction cell.

FIG. 2 is a cross section of a back-contacted cell having both front and back junctions.

DETAILED DESCRIPTION OF THE INVENTION

Several versions of the basic cell will be presented below. At its simplest, the cell may be characterized as a back-contacted front-junction cell. This cell may also have a back-junction as an added element. There are several methods by which these cells can be made, and variations of those specifically discussed herein are possible. The reader should refer to the claims to determine the true scope of this invention.

FIG. 1 is an isometric view of a portion of a back-contacted cell with a front junction. FIG. 2 is a cross-sectional view of a similar cell with the addition of a back junction.

One of the paths to constructing a back-contacted cell with a front junction is as follows: First, phosphorus is diffused into the top surface 12 of the cell 10 to achieve a sheet resistance of about 100Ω/□ in front emitter region 22. The main substrate body 24 of the cell is bulk p-type silicon. Next, a dielectric layer, not shown, is either grown (SiO_2) or deposited (Si_3N_4 or other materials) on both surfaces. A laser is then used to scribe a first set of grooves 16 and drill holes

(vias) **20** on the back surface **14**. These grooves and vias are subsequently etched and heavily diffused with phosphorus (n^{++}). The phosphorus diffusion on the via walls **25** serves as an electrical conduction path between the phosphorus diffusion region **22** on the front surface **12** and a subsequently deposited grid on the back surface **14**. For embodiments where metal is deposited inside the via **20**, the phosphorus diffusion along the via walls **25** also electrically isolates the metal in the via from the p-type substrate.

Next, a p-type contact **18** to the substrate **24** is formed that is interdigitated with the aforementioned n^{++} grooves and vias. Several options exist for forming the interdigitated contact to the p-type substrate **24**. One option is to preform a patterned aluminum alloy layer using the well-known art of screen printing an aluminum paste and alloying the paste to form a heavily doped p-type region **26**. The aluminum may be alloyed through the dielectric or the dielectric may be removed from the p-type contact region **18** prior to the aluminum deposition. One means of selectively removing the dielectric is to again use a laser or use a dicing saw to scribe a second set of grooves **26** that is interdigitated with the first set of grooves **28**. The second option uses a boron diffusion to form the heavily doped, p-type region **26**; this option also requires a laser or dicing saw to form a second set of grooves **28** that are interdigitated with the first set of grooves **16**. Note that the n^{++} grooves **16** and vias **20** must be protected from boron during the boron diffusion, which can be done with either an oxide grown during the preceding phosphorus diffusion or with a SiO_2 deposition after the preceding phosphorus diffusion.

The next step is to deposit metal grids over the n-type and p-type contacts. On method to form this metallization is to first deposit a thin layer of nickel in the groove(s) by electroless deposition, sinter the nickel with the silicon to form a low resistance contact, and plate a thick layer of either silver or copper to make a high-conductance grid. The dielectric layer in this embodiment acts as an etch stop during the groove etch(es), as a diffusion mask during the diffusion(s), as a plating mask during the metallization step, and as the antireflection coating in the finished cell. A related process is described for the fabrication of solar cells with diffused, metalized grooves on the front surface in M. A. Green, et al., 22nd IEEE Photovoltaic Specialists Conference, pg. 46 (1991), and in U.S. Pat. Nos. 4,726,850 and 4,748,130 to S. R. Wenham and M. A. Green, which are incorporated herein by reference in their entireties.

A variation of the above process sequence forms the p-type contact before rather than after the n-type grooves and vias. A particularly convenient sequence diffuses the boron into the p-type contact region at the same time as the heavy phosphorus diffusion is performed to dope the n-type contact grooves and vias. This sequence starts with a p-type silicon substrate. A light (around 100Ω/□) phosphorus diffusion is performed over the front surface and a dielectric is grown or deposited over both surfaces. Next, a laser, dicing saw, or patterned etch is used to form grooves for the p-type contact **18**. These grooves are etched and borosilicate glass is deposited by chemical vapor deposition on the back surface. Next, n-type grooves **16** and vias **20** are scribed on the back surface **14** with a laser for the n-type contact region. These grooves are interdigitated with the p-type grooves. These grooves and vias are etched and then heavily diffused with phosphorus. Boron diffuses from the borosilicate glass during the phosphorus diffusion to dope the p-type contact region. Alternatively, a conventional boron diffusion could be performed in place of the borosilicate glass deposition, so that the p-type diffusion is formed in a separate furnace step than the n-type contact. The cell is completed by plating metal to form the grids as previously described.

A variation of the basic cell is shown in FIG. 2. This cell has carrier-collection junctions on both the front and back surfaces. The phosphorus diffusion creates the front emitter **22** and the additional back emitter **23** in the same step. Heavy boron diffusion, or an aluminum alloy, is done to contact the bulk **24**. The diffusion length only needs to be half the width of the cell for good collection efficiency with junctions on both surfaces, which would allow the use of inexpensive, poor quality silicon substrates.

The above-described processes can produce a quite efficient cell but one which might be somewhat expensive due to the use of several high temperature steps. The above process normally requires at least three furnace steps above 800° C. for the n^+ diffusion, n^{++} groove diffusion, and the p^{++} aluminum-alloyed or boron-diffused p-type contact emplacement. Silicon nitride for the dielectric and metal plating (nickel and silver or copper) for the metallization are also required. In contrast, commercially produced solar cells, although less efficient, use lower cost screen-printed grids and a single furnace step above 800° C. for the n^+ diffusion.

Processes based on these commercial techniques can also be used to produce a more economical, although somewhat less efficient, version of the back-contact solar cell of this invention. Such a production process would include the following steps. The surfaces of the p-type substrate would be prepared by cleaning and texturing, followed by laser drilling and etching the via holes. This would be followed by a phosphorus diffusion step to achieve a sheet resistance level of about 50 Ω/□. This step forms an n+ diffusion on the front and back surfaces and inside the via. Next would be a PSG (phosphorsilicate glass) removal step followed by the deposition of an antireflective coating on the front surface. On the back, a grid of Ag paste would be screen printed and fired. This grid is aligned to the vias and forms the n^+ contacts and the associated grid. Next, an AlAg paste would be screen printed onto the back and fired to form the p^+ contacts and the associated grid.

It is this last step that can present the most difficulty. The AlAg paste must alloy through the phosphorus diffusion on the back to make contact to the p-type substrate without forming a shunted junction with the adjacent n+ diffusion. Other options for forming the p-type contact include the following: remove a region of the n^+ diffusion by scribing (laser or saw) or patterned chemical etch process prior to the AlAg past application; isolate the p-type contact from the n^+ diffusion after firing of the AlAg paste by scribe or chemical etch process; or first fire an Al paste to obtain an alloyed junction with high quality and subsequently print Ag paste to form the conductive grid. Hitachi has used a chemical etch after AlAg paste firing to make a double-junction emitter cell. They reported an efficiency of 18.8% for a large-area multicrystalline silicon solar cell using the above sequence without the laser holes and with a grid on the front surface. T. Warabisako, K. Matsukuma, S. Kokunai, J. Kida, T. Uematsu, H. Ohtsuka and H. Yagi, "A 16.8% Efficient, 100CM^2 Polycrystalline Silicon Solar Cell With Triode Structure," 11th E.C. Photovoltaic Solar Energy Conference, 12–16 October 1992, Montreux, Switzerland.

This commercial-process back-contact cell has a somewhat lower potential performance than the back-contact cell previously described because of the single diffusion. The sheet resistance of the single diffusion is a compromise between low series resistance (particularly contact resis-

tance to the screen-printed metallization) and good blue wavelength response. It is anticipated that the optimal sheet resistance to achieve this compromise is near the 50 Ω/□ value presented above. The process of the first embodiment avoids this compromise by using separate diffusions for the illuminated region and for the contact region. The compromise value for the sheet resistance in the second embodiment will probably result in lower blue response, higher contact resistance, and larger emitter recombination. This compromise could be improved by etching back the front diffusion. This variation would still use a single diffusion but would obtain different sheet resistances on the front and back surfaces. The front-surface diffusion after etching would be more optimal for blue response, while the back-surface diffusion would be more optimal for contact resistance and emitter recombination. This variation would require a simple means to mask the vias and the back from the etch.

The reader will understand that n-type silicon substrates can be substituted for p-type substrates with corresponding reversals in the conductivity types of the various regions in the cell as compared with the descriptions above. In the claims below, this interchangeability between the two conductivity types is at times indicated by the generic terminology: "one conductivity type" and "the other conductivity type."

I claim:

1. A method for making a back-contacted photovoltaic cell, comprising:

diffusing phosphorus into the front surface of a planar p-type silicon substrate to achieve a sheet resistance of about 100 ω/□;

forming a dielectric layer on top of the phosphorus diffusion and on the back surface of the substrate;

laser scribing a first set of spaced apart grooves into the back surface and laser drilling an array of holes through the substrate to form vias such that portions of the first set of grooves are proximate to the holes;

diffusing phosphorus into the vias and the first set of grooves;

forming a second set of spaced apart grooves interdigitated with the first set;

metallizing the vias and the first and second sets of grooves; and

forming separate electrical contacts to the metallizations over the first and second sets of grooves.

2. The method of claim 1 further including the step of diffusing phosphorus into the back surface of the substrate prior to the formation of the dielectric layer.

3. The method of claim 2 further including a separate step of introducing a p-type impurity onto the back surface of the substrate in the second set of grooves to form a bulk-contact diffusion zone prior to metallizing the second set of grooves.

4. The method of claim 3 wherein the p-type impurity is introduced by depositing borosilicate glass on the back surface.

5. The method of claim 3 wherein the p-type impurity is introduced by diffusing boron into the second set of grooves.

6. A method for making a back-contacted photovoltaic cell, comprising:

diffusing phosphorus into the front surface of a planar p-type silicon substrate to achieve a sheet resistance of about 100 Ω/□;

forming a dielectric layer on top of the phosphorus diffusion and on the back surface of the substrate;

forming a first set of spaced apart grooves in the back surface to communicate with a p-contact grid;

etching the first set of grooves;

introducing boron impurities into the first set of grooves;

laser scribing a second set of spaced apart grooves interdigitated with the first set into the back surface and laser drilling an array of holes through the substrate to form vias such that portions of the second set grooves are proximate to the holes;

diffusing phosphorus into the vias and the second set of grooves;

metallizing the vias and the first and second sets of grooves; and

forming separate electrical contacts to the metallizations over the first and second set of grooves.

7. A method for making a back-contacted photovoltaic cell, comprising:

laser drilling an array of holes through a planar silicon substrate of one conductivity type;

diffusing an impurity of the other conductivity type into the holes and the front and back surfaces of the substrate;

depositing an antireflective coating onto the front surface of the substrate;

screen printing a first paste containing a conductive metal onto the back surface of the substrate, overlapping the holes and forming a first grid thereon, and then firing the the pasted substrate; and

screen printing a second paste which contains a conductive metal and is capable of forming a contact with the underlying substrate through the region on the back surface into which the diffusion of the conductivity type has been made and firing the substrate to form a second grid.

8. The method of claim 7 further including removing a portion of the diffused region from the back surface and then screen printing the second paste into this portion.

9. The method of claim 7 further including removing a portion of the diffused region on the back surface after screen printing of the second paste to isolate the second-paste region from the diffused region.

10. The method of claim 7 further including the step of etching away a portion of the diffused region on the front surface of the substrate.

11. The method of claim 7 wherein the second paste has at least two components, one of which is capable of alloying with the underlying substrate and one which is a conductive metal.

12. The method of claim 11 wherein the one conductivity type is p-type, the opposite conductivity type is n-type, the conductive metal is Ag, and the alloying component is Al.

13. A method of forming a photovoltaic cell, comprising:

laser drilling an array of holes through a planar silicon substrate of one conductivity type;

diffusing an impurity of the opposite conductivity type into the holes and the front and back surfaces of the substrate;

depositing an antireflective coating onto the front surface of the substrate;

screen printing a first paste containing a conductive metal onto the back surface of the substrate, overlapping the holes and forming a first grid thereon, and then firing the pasted substrate;

screen printing a second paste containing an alloying

component capable of forming a contact, through a portion of the region on the back surface into which the diffusion of the opposite conductivity type has been made, with the underlying substrate; and

screen printing a third paste containing a conductive metal over the second paste and firing the pasted substrate to form a second grid.

14. The method of claim 13 further including the step of etching away a portion of the diffused region on the front surface of the substrate.

15. The method of claim 13 wherein the one conductivity type is p-type, the opposite conductivity type is n-type, the conductive metal is Ag, and the alloying component is Al.

* * * * *

US006836020B2

(12) **United States Patent**
Cheng et al.

(10) **Patent No.: US 6,836,020 B2**
(45) **Date of Patent: Dec. 28, 2004**

(54) **ELECTRICAL THROUGH WAFER INTERCONNECTS**

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(73) Assignee: **The Board of Trustees of the Leland Stanford Junior University**, Stanford, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **10/349,597**

(22) Filed: **Jan. 22, 2003**

(65) **Prior Publication Data**

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(52) **U.S. Cl.** **257/774**
(58) **Field of Search** 257/774, 618, 257/595, 496, 602

(56) **References Cited**

U.S. PATENT DOCUMENTS

5,619,476 A	*	4/1997	Haller et al.	367/181
5,870,351 A	*	2/1999	Ladabaum et al.	367/163
5,894,452 A	*	4/1999	Ladabaum et al.	367/163
6,430,109 B1	*	8/2002	Khuri-Yakub et al.	367/181
6,674,126 B2	*	1/2004	Iwamoto et al.	257/341

OTHER PUBLICATIONS

Alizadeh-Taheri, B., et al., "An Active, Microfabricated, Scalp Electrode-Array for EEG Recording", *Transducers '95—Eurosensers IX*, The 8th International Conference on Solid-State Sensors and Actuators, and Eurosensors IX, Stockholm, Sweden, Jun. 25–29, 1995, pp. 67–70.

Bollmann, D., et al., "Invited paper: Three Dimensional Metallization for Vertically Integrated Circuits", *Materials for Advanced Metallization*, 1997, pp. 94–98.

Burger, G.J., et al., "High Resolution Shadow Mask Patterning in Deep Holes and Its Application to an Electrical Wafer Feed-Through", *Transducers '95—Eurosensors IX*, The 8th International Conference on Solid-State Sensors and Actuators, and Eurosensors IX. Stockholm, Sweden, Jun. 25–29, 1995, pp. 573–576.

Calmes, S., et al., "Highly Integrated 2-D Capacitive Micromachined Ultrasonic Transducers", 1999 IEEE Ultrasonics Symposium, *IEEE*, 1999, pp. 1163–1166.

Cheng, C.H., et al., "An Efficient Electrical Addressing Method Using Through-Wafer Vias for Two-Dimensional Ultrasonic Arrays", 2000 IEEE Ultrasonics Symposium, *IEEE* , 2000, pp. 1179–1182.

Christensen, C., et al., "Wafer Through-Hole Interconnections with High Vertical Wiring Densities", *IEEE*, Dec. 1996, 19(4):516–522.

Fujita, Y., et al., "Feasibility Study on Through-Wafer Interconnecting Method for Hybrid Wafer-Scale -Integration", *IEEE*, 1999, pp. 1081–1084.

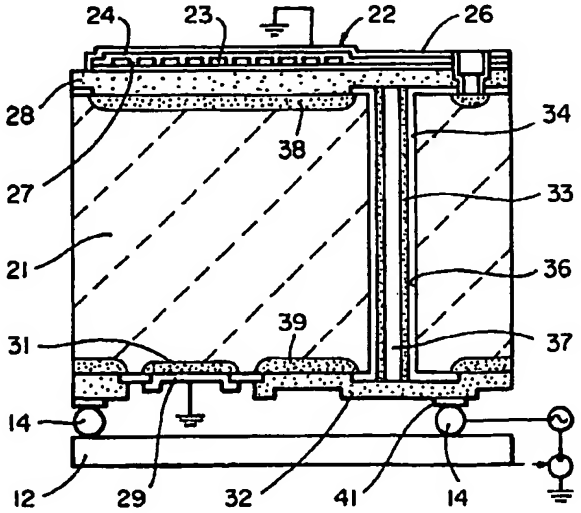
(List continued on next page.)

Primary Examiner—Roy Potter
(74) *Attorney, Agent, or Firm*—Dorsey & Whitney LLP

(57) **ABSTRACT**

A wafer with through wafer interconnects. The wafer includes spaced through wafer vias which extend between the back side and front side of the wafer. A conductor within each of said vias connects to front and back side pads. Functions associated with said conductor and said pads provide a depletion region in the wafer between the pads and wafer or pads and conductor and the wafer.

20 Claims, 6 Drawing Sheets



OTHER PUBLICATIONS

Heschel, M., et al., "Conformal Coating By Photoresist Of Sharp Corners Of Anisotropically Etched Through–Holes In Silicon", *Transducers '97*, 1997 International Conference on Solid–State and Actuators, Chicago, Jun. 16–19, 1997, pp. 209–212.

Li, X., et al., "High Density Electrical Feedthrough Fabricated by Deep Reactive Ion Etching of Pyrex Glass", *IEEE*, 2001, pp. 98–101.

Linder, S., et al., "Fabrication Technology for Wafer Through–Hole Interconnections and Three–Dimensional Stacks of Chips and Wafers", *IEEE*, 1994, pp. 349–354.

Little, M.J., et al., "The 3–D Computer", *IEEE*, 1989, pp. 55–72.

Liu, C., et al., "Through–Wafer Electrical Interconnects by Sidewall Photolithographic Patterning", *IEEE*, 1998, pp. 1402–1405.

Kuhmann, J.F., et al., "Through Wafer Interconnects and Flip–Chip Bonding: A Toolbox for Advanced Hybrid Technologies for MEMS", *Eurosensors XIII*, The 13th European Conference on Solid–State Transducers, Sep. 12–15, 1999, The Hague, The Netherlands, pp. 265–272.

Mita, Y., et al., "Two Dimensional Micro Conveyance System with Through Holes for Electrical and Fluidic Interconnection", *Transducers '97*, 1997 International Conference on Solid–State Sensors and Actuators, Chicago, Jun. 16–19, 1997, *IEEE*, 1997, pp. 37–40.

Nguyen, N.T., et al., "Through–wafer copper electroplating for three–dimensional interconnects", *J. Micromech. Microeng.*, 2002, 12:395–399.

Takahata, K., et al., "Batch Mode Micro–EDM for High–Density and High–Throughput Micromachining", *IEEE*, 2001, pp. 72–75.

Wu, J.H., et al., "A High Aspect–Ratio Silicon Substrate–Via Technology and Applications: Through–Wafer Interconnects for Power and Ground and Faraday Cages for SOC Isolation", *IEEE*, 2000, pp. 477–480.

Kallis, J.M., et al., "Reliability of the 3–D Computer Under Stress of Mechanical Vibration and Thermal Cycling", IEEE, 1989, pp. 65–72.

* cited by examiner

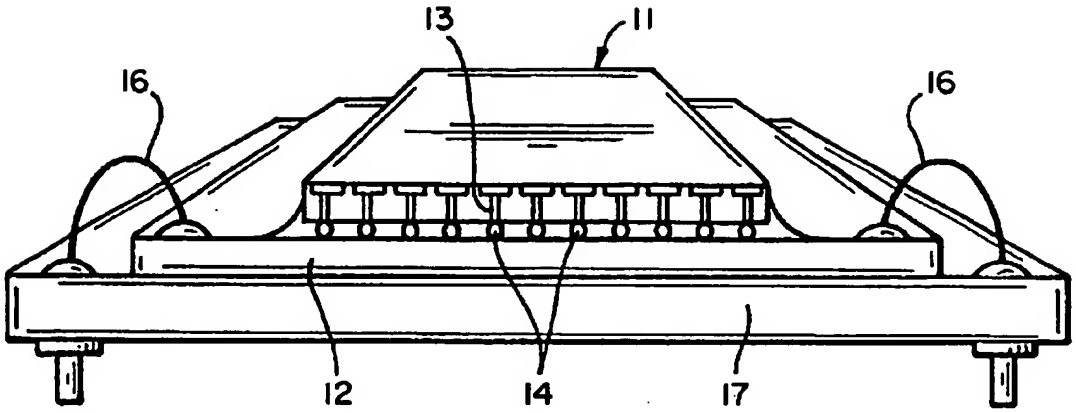

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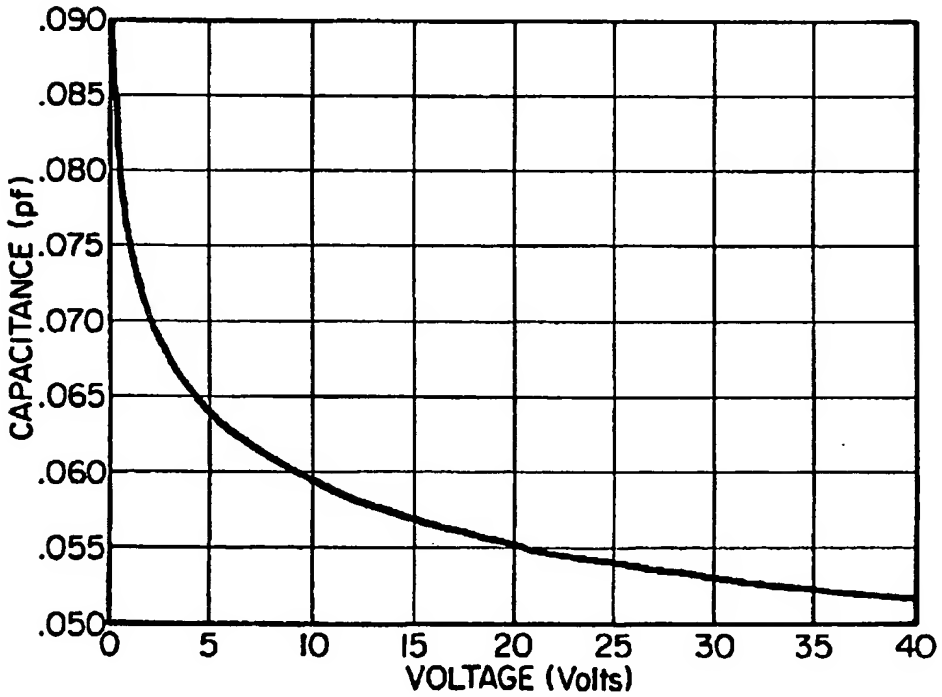
FIG_1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.070
.065
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.055
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CAPACITANCE (pf)
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5
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15
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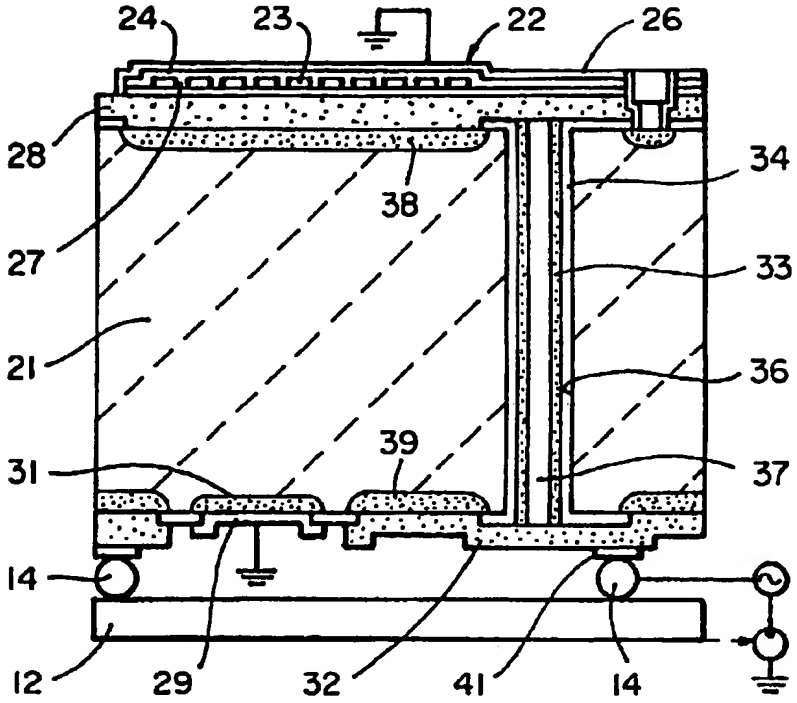
25
30
35
40
VOLTAGE (Volts)

FIG_6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41
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FIG_2

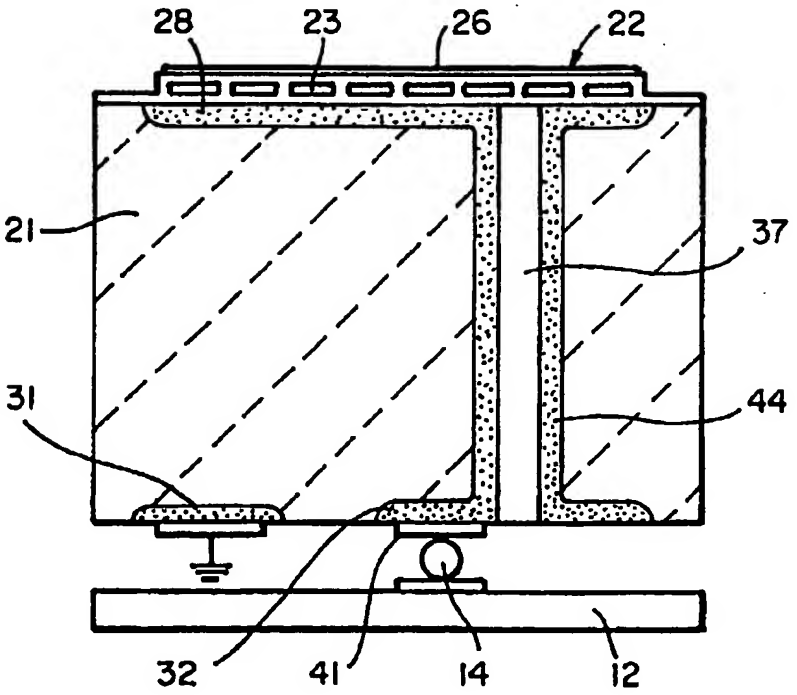
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FIG_3

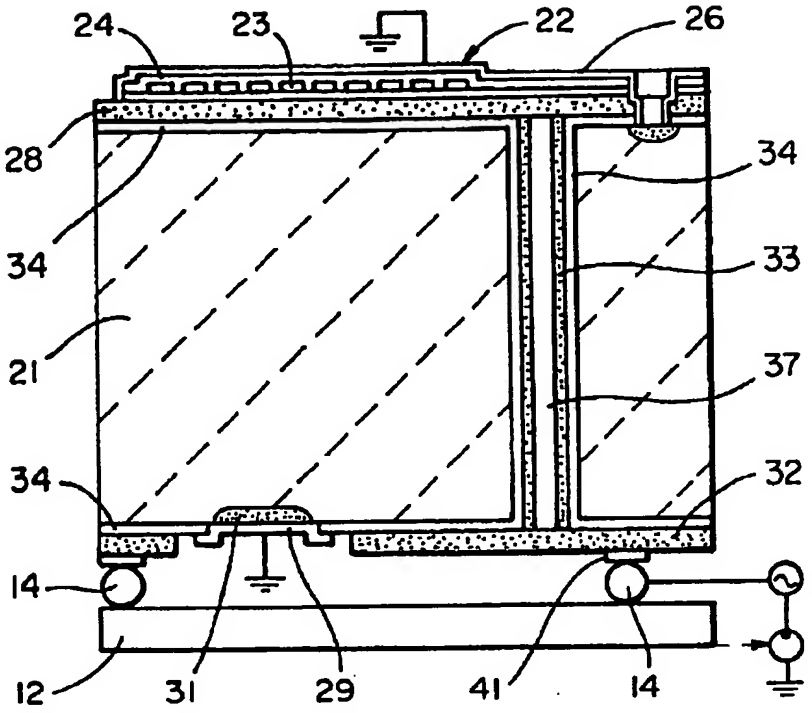
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FIG_4

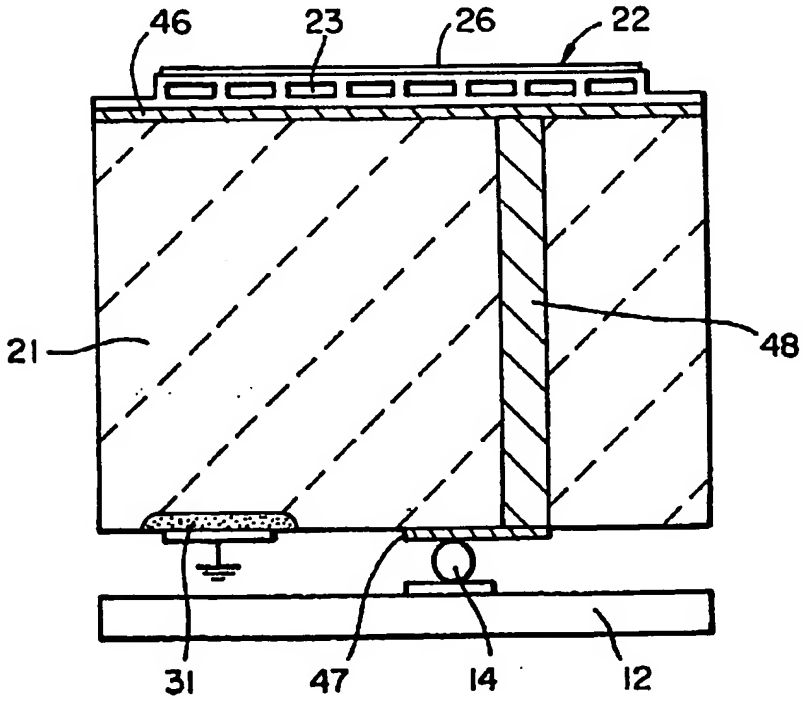
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FIG_5

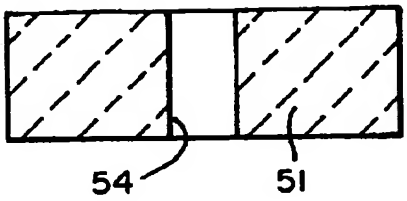

FIG_7a

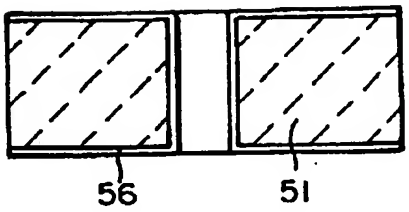

FIG_7b

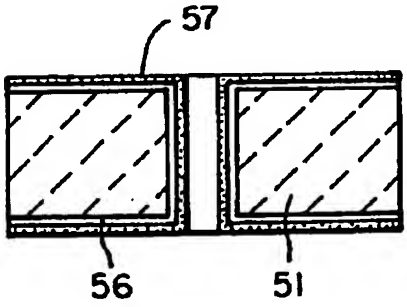

FIG_7c

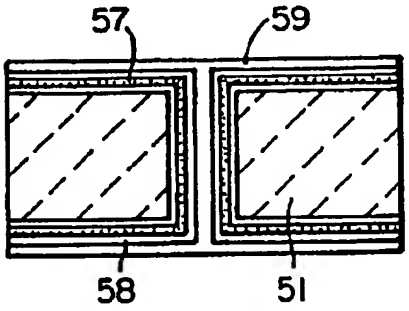

FIG_7d

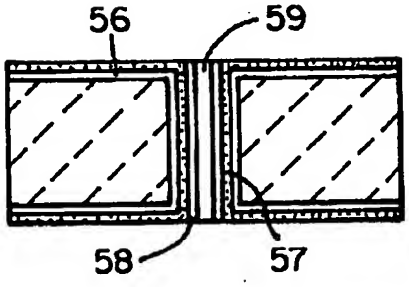

FIG_7e

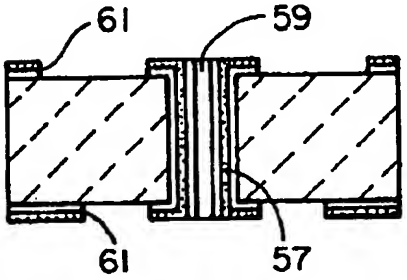

FIG_7f

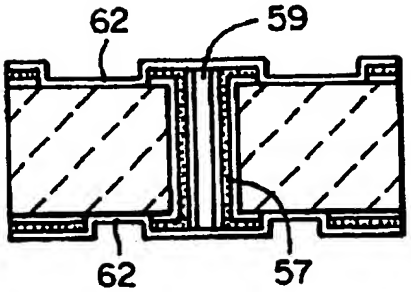

FIG_7g

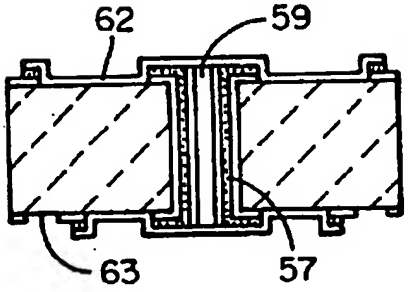

FIG_7h

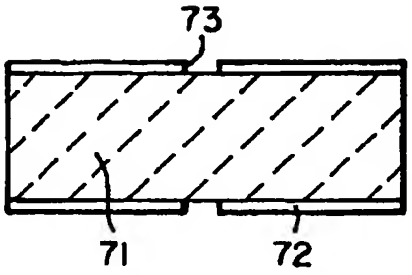

FIG_8a

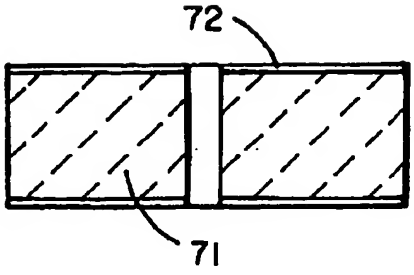

FIG_8b

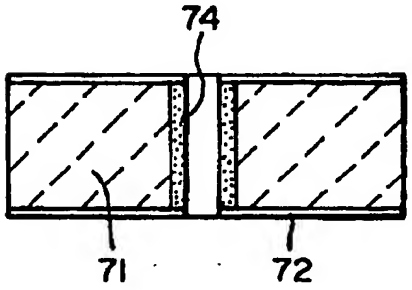

FIG_8c

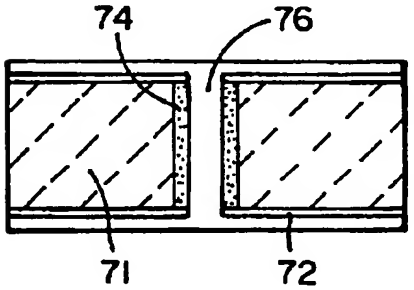

FIG_8d

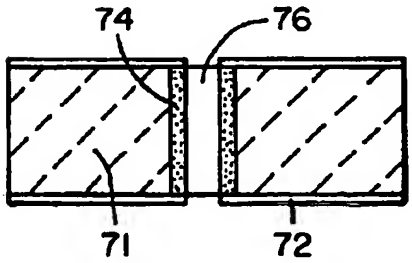

FIG_8e

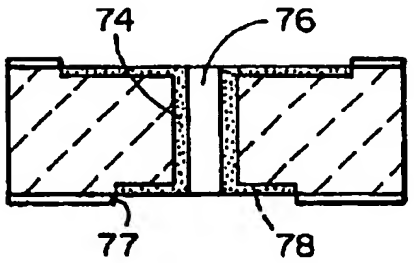

FIG_8f

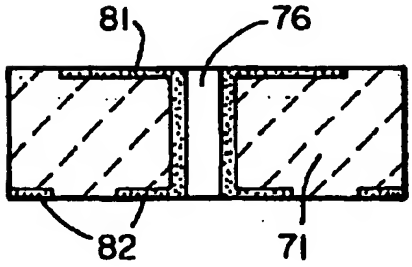

FIG_8g

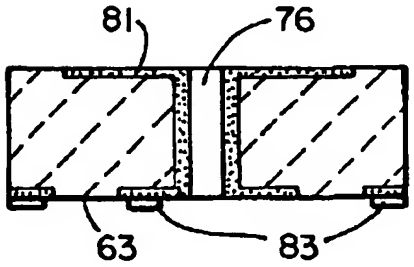

FIG_8h

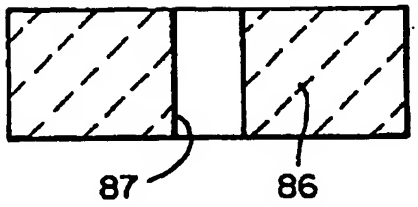

FIG_9a

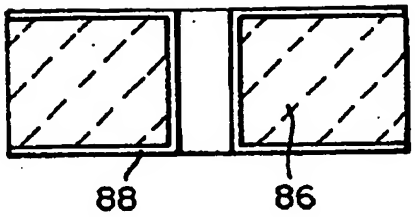

FIG_9b

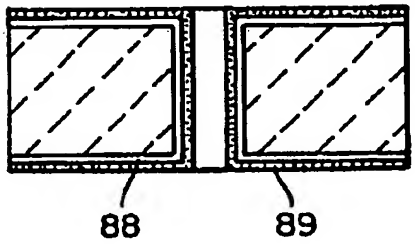

FIG_9c

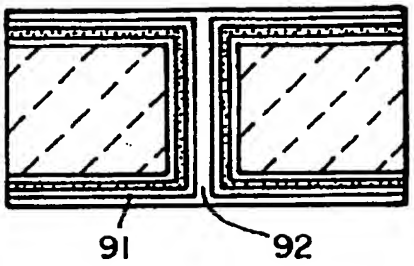

FIG_9d

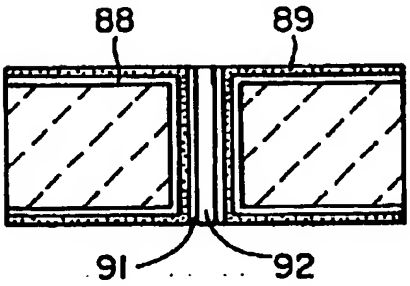

FIG_9e

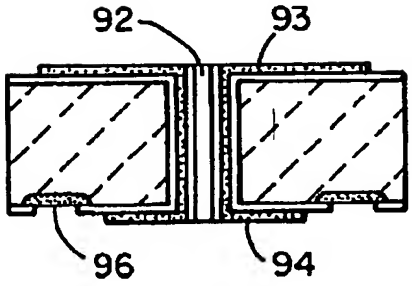

FIG_9f

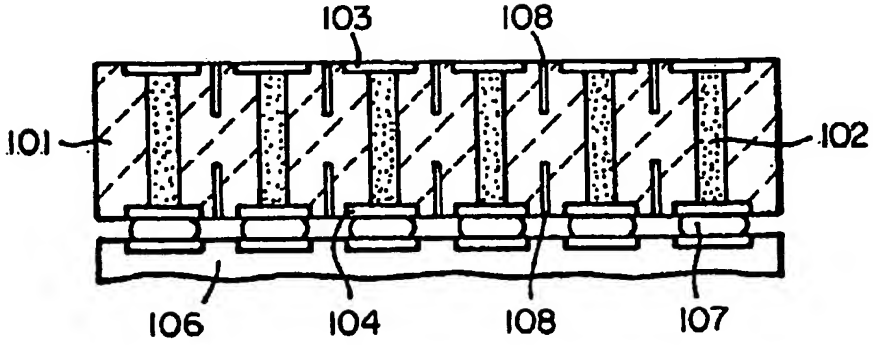

FIG_10

ELECTRICAL THROUGH WAFER INTERCONNECTS

GOVERNMENT SUPPORT

This invention was made with Government support under Contract No. N00014-98-0634 awarded by the Department of the Navy, Office of Naval Research. The Government has certain rights in this inventiom.

BRIEF DESCRIPTION OF THE INVENTION

This invention relates generally to electrical through wafer interconnects and more particularly to through wafer interconnects in which the parasitic capacitance is minimized.

BACKGROUND OF THE INVENTION

In co-pending application Ser. No. 09/667,203 filed Sep. 21, 2000, there is described an ultrasonic transducer with through wafer connections. Capacitive micro machined ultrasonic transducer arrays include membranes which are supported on the front side of a substrate or wafer by isolator supports such as silicon nitride, silicon oxide and polyimide. Transducers of this type are described, for example, in U.S. Pat. Nos. 5,619,476; 5,870,351; and 5,894,452. Micromachined two-dimensional arrays of droplet ejectors which include a flexible membrane supported on a substrate are described, for example, in U.S. Pat. No. 6,474,786. Other two-dimensional device arrays such as for example, arrays of vertical cavity surface emitting lasers, mirrors, piezoelectric transducers, photo detectors and light emitting diodes are formed on and supported by the front side of wafers or substrates.

One of the main problems in fabricating two dimensional arrays is that of addressing the individual array elements. If the array size is large, a significant sacrifice in the array element area is required if the addressing is done through a routing network on the top side of the substrate. The interconnect between the array elements and their electronics gives rise to parasitic capacitance which limits the dynamic range and frequency bandwidth of the device array. It is therefore advantageous to have the electronic circuitry as close to the array elements as possible. However, integrating the devices, the electronics and the interconnects on the same wafer leads to a compromise in the performance of both the electronics and the device array.

An excellent solution to the problem is to fabricate separately the optimum device array and the electronics, provide through wafer interconnects with high aspect ratio and the flip chip bond the wafer to the electronics. This also provides a lower parasitic capacitance between the electronic circuit and the array elements. However it is desirable to further reduce the parasitic capacitance.

OBJECTS AND SUMMARY OF THE INVENTION

In accordance with the invention, the reduction in parasitic capacitance is achieved by employing reverse biased pn, Schottky junctions, or MIS (Metal Insulator Semiconductor) biasing to depletion in the interconnects.

It is an object of the present invention to provide a wafer with through wafer interconnects with a low parasitic capacitance and resistance.

It is a further object of the present invention to provide a wafer which includes front side and back side pads and a through wafer interconnect with low parasitic capacitance and resistance.

There is provided a wafer with through wafer interconnect. The wafer included spaced through wafer vias which extend between the back side and front side of the wafer, a conductor within each of the vias connected to front and back side pads and means associated with said conductor and pads and the wafer for providing a depletion region in the wafer between the conductor and pads.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention will be more clearly understood from the following description when read in conjunction with the accompanying drawings in which:

FIG. **1** is a perspective view of micromachined devices (MEMS) with through wafer interconnects;

FIG. **2** is a sectional view showing a wafer with a through wafer interconnect in accordance with our embodiment of the present invention;

FIG. **3** is a sectional view showing a wafer with a through wafer interconnect in accordance with still a further embodiment of the present invention;

FIG. **4** is a sectional view showing a wafer with a through wafer interconnect in accordance with still another embodiment of the present invention;

FIG. **5** is a sectional view showing a wafer with a through wafer interconnect in accordance with still another embodiment of the present invention;

FIG. **6** is a curve showing the expected capacitance-voltage relationship for a pn junction interconnect;

FIG. **7** shows the process steps for fabricating a wafer with through wafer MIS vias and pn-junction pads;

FIG. **8** shows the process steps for fabricating a wafer with through wafer interconnect with pn junction vias and pads;

FIG. **9** shows the process steps for fabricating a wafer with through wafer interconnect with MIS vias and pads;

FIG. **10** schematically shows a wafer with through wafer interconnects with trenches for reduction of thermal mismatch between the device array and the electronics.

DESCRIPTION OF PREFERRED EMBODIMENTS

FIG. **1** shows MEMS devices **11** connected to integrated circuits **12** with through wafer interconnects **13** and solder bumps **14**. The integrated circuit (electronics) **12** is shown wire bonded **16** to a printed circuit board **17**. The MEMS array is connected with the electronic circuits without sacrificing the performance of either one and minimizing the parasitic capacitance. In transducer array operation the parasitic capacitance of the interconnect between an array element and its electronics is the limiting factor for the dynamic range and frequency bandwidth. Therefore, it is always best to put the electronics as close to the array elements as possible. To do this, an electrical through wafer interconnect (ETWI) is employed to address the array elements individually, where the front side of the wafer is fully populated with the array elements and the backside is solely dedicated to bond pads for the flip-chip bonding to the printed circuit board (PCB) or the integrated circuits as shown in FIG. 1. In this way, the parasitics due to any interconnection cable or traces are avoided. To further improve the device performance, the parasitic capacitance of the ETWI to the silicon substrate needs to be reduced to a comparatively lower level than the device capacitance. For each array element, there are three sources contributing to

the parasitic, the front side pad for the transducers, the back side pad for the bonding, and the through wafer interconnect.

One of the solutions for the parasitic reduction is to implement reverse-biased pn junction on the front and backside pads of the wafer and an MIS junction interconnects. Referring to FIG. **2**, a small section of a wafer **21** is shown with one ultrasonic transducer **22** formed on the front side of the wafer. The transducer includes active cells **23**, which comprise flexible membranes **24** having a top (ground) electrode **26** supported by insulating supports **27** and a bottom signal electrode **28**. A detailed description of the fabrication of ultrasonic transducers is found in the above-referenced patents which are incorporated herein in their entirety by reference. The top electrode is connected to ground **29** through ohmic contact **31** with the wafer **21**. The bottom electrode **28** comprises the top side pad and is connected to the back side pad **32** by via conductor **33** formed on the oxide layer **34** grown in the via **36**. The via may be sealed by polysilicon filler **37**. Diffusion regions **38** and **39** are formed in the wafer or substrate **21** and define pn junctions which can be reverse biased by applying a dc voltage to the interconnect and pads to provide a depletion layer. When the pn junctions are reverse biased, the high resistivity (>1000 ohm-cm) silicon substrate is fully depleted achieving a low parasitic capacitance at the top side and back side pads. The back side pads are connected to the processing or integrated circuit **12** by solder pads **41** and solder bumps **14**.

Another solution for parasitic capacitance reduction is to implement reverse biased pn-junction diodes inside the interconnects as well as at the pads as shown in FIG. **3**. In FIG. **3** parts like those in FIG. **2** have the same reference numbers and are not further described. The front side pads **28**, back side pads **32** and the through via interconnects **44** comprise highly doped regions which serve as the conductors. The regions form pn junctions which can be reverse biased.

When a reverse bias dc voltage is applied to the pn junction, the high resistivity (>1000 ohm-cm) silicon substrate is fully depleted from electrons, thus a low parasitic capacitance is achieved.

As an example let us consider a top side 400 m×400 m pad, a 140 m×200 m back side pad, a 20 m diameter via and a 400 m thick wafer having a resistivity of 1000 ohm-cm with a reverse biased voltage driving the junction diode into the depletion region. The expected capacitance-voltage relationship is show in FIG. **6**. We expect the total parasitic capacitance to be lower that 0.06 pF for a reverse bias voltage of more than 10 volts. This includes capacitance of the front and backside pads and a single through-wafer interconnect. This is a substantial improvement over previously reported results. The predicted series resistance is 434 which assumes that the doping profile is the same for the surfaces on top of the wafer and inside the via holes.

Another solution for parasitic capacitance reduction is to implement MIS junction inside the interconnects at the pads as well as inside the interconnects as shown in FIG. **4**. The MIS junction will give a better electrical isolation for high voltage applications. It will also give certain amount of parasitic capacitance reduction when biasing to depletion although not as good as using reverse-biased pn junction. In FIG. **4** parts like those in FIG. **2** have the same reference numbers and are not further described. The front side pads **28**, back side pads **32** and the through via interconnects **33** comprise doped polysilicon which serve as the conductors. The regions form MIS junction which can be biased to depletion. When the MIS junctions are biased to depletion, the high resistivity (>1000 ohm-cm) silicon substrate is depleted to certain width (>9 m)achieving a low parasitic capacitance at the via, the top side, and the back side pads.

Another solution for the parasitic reduction is to implement reverse-biased Schottky diodes on the front and backside pads of the wafer and inside the interconnects as shown in FIG. **5**. The top side, back side pads **47** and **46**, interconnect **48** are a metal which form Schottky junctions with the substrate. Like reference numbers have been applied to parts like in FIGS. **2** and **3**. With a reverse bias dc voltage applied to the Schottky diode, the high resistivity (>1000 ohm-cm) silicon substrate is fully depleted of electrons. Thus a low capacitance is achieved.

The process flow for forming a wafer with through wafer interconnects of the type shown in FIG. **2** is shown in FIG. **7**. We start with a 400 μm thick double-sided polished silicon wafer **51** which is thermally oxidized to 2 μm thick to serve as a hard mask for the deep etch. Both sides are then patterned with 20 μm diameter openings for each interconnect. A through-wafer deep etch is done by etching halfway from both sides of the wafer (FIG. **7***a*). By this means, a 20 to 1 high aspect ration via hole **54**, can be achieved. The oxide mask is then removed by buffered oxide etch (BOE). For MIS isolation, interconnect side walls and wafer front and backside pads are grown with 1 μm of thermal oxide **56** (FIG. **7***b*). A layer **57** of 2 μm polysilicon is deposited and then heavily doped with boron or phosphorous depending on the wafer type to enhance the conductance (FIG. **7***c*). A layer **58** of low temperature oxide (LTO) is deposited to serve as an etching stop for the etch-back of polysilicon deposited in the following step. The interconnect holes are then filled with polysilicon **59** (FIG. **7***d*). The polysilicon on both sides is then etched back and stopped on the LTO (FIG. **7***e*). After removing the LTO, the 2 μm doped polysilicon is exposed again and ready to be etched for the front and back side oxide opening **61** (FIG. **7***f*). Another layer **62** of 0.5 μm polysilicon is deposited and doped with boron or phosphorous (FIG. **7***g*). The front and back side polysilicon pads are patterned followed by the oxide etch on the back side for ground opening **63** and heavily doped for ohmic contact. After this step, the array of devices can be built on top of the front side polysilicon.

The process flow for fabricating a wafer with through wafer interconnects of the type shown in FIG. **3** is shown in FIG. **8**. We start with a 400 μm thick double-sided polished Si wafer **71** which is thermally oxidized to 2 μm thick **72** to serve as a hard mask for the deep etch. Both sides are then patterned with 20 μm diameter openings **73** for each interconnect (FIG. **8***a*). The through-wafer deep etch is done by etching half way from both sides of the wafer (FIG. **8***b*). By this means, a 20 to 1 high aspect ratio via hole can be achieved. The wafer is then heavily doped with boron or phosphorous **74** depending on the wafer type to build the pn junction diode inside the holes (FIG. **8***c*). The interconnect holes are then filled with polysilicon **76** (FIG. **8***d*). The polysilicon on both sides is then etched back and stopped on the oxide (FIG. **8***e*). It is ready to be etched for the front and back side oxide opening **77** (FIG. **8***f*). The wafer is then doped with boron **78** which makes up the pn junctions for the front and back side pads **81**, **82**. The oxide is etched on the back side for ground opening **63** and heavily doped for ohmic contact **83**. After this step, the array of devices can be built on top of the front side pn junction pad.

The process flow for forming a wafer with through wafer interconnects of the type shown in FIG. **4** is shown in FIG.

9. We start with a 400 m thick double-sided polished silicon wafer **86** which is thermally oxidized to 2 m thick to serve as a hard mask for the deep etch. Both sides are then patterned with 20 m diameter openings for each interconnect. A through-wafer deep etch is done by etching halfway from both sides of the wafer (FIG. 9*a*). By this means, a 20 to 1 high aspect ration via hole **87**, can be achieved. The oxide mask is then removed by buffered oxide etch (BOE). For MIS isolation, interconnect side walls and wafer front and backside pads are grown with 1 m of thermal oxide **88** (FIG. 9*b*). A layer **89** of 2 m polysilicon is deposited and then heavily doped with boron or phosphorous to enhance the conductance (FIG. 9*c*). A layer **91** of low temperature oxide (LTO) is deposited to serve as an etching stop for the etch-back of polysilicon deposited in the following step. The interconnect holes are then filled with polysilicon **92** (FIG. 9*d*). The polysilicon on both sides is then etched back and stopped on the LTO (FIG. 9*e*). After removing the LTO, the 2 m doped polysilicon is exposed again and ready to be etched for the front and back side pads **93, 94** patterning (FIG. 9*f*). The oxide is opened on the back side for ground opening **96** and heavily doped for ohmic contact. After this step, the array of devices can be built on top of the front side polysilicon.

Referring to FIG. **10**, a wafer **101** with through via interconnects **102** and top side and bottom side pads **103** and **104** is schematically shown. This wafer is flip chip bonded to a integrated or processing circuit **106** or to a printed circuit board by solder bumps **107**. Trenches **108** are etched in the wafer to reduce lateral stiffness at the surface of the wafer. Stress induced by thermal expansion differences between the wafer and associated connected devices is reduced, extending the lifetime of the assembly by reducing fatigue due to the thermal expansion differences.

A wafer with high density and low parasitic capacitance electrical through-wafer interconnects (vias) for connection to an array of micromachined transducers or devices on a silicon wafer has been described. The wafer provides vertical wafer feedthroughs (interconnects) connecting an array of sensors or actuators from the front side (transducer side) to the backside (packaging side) of the wafer. A 20 to 1 high aspect ratio 400 μm long and 20 μm diameter interconnect is achieved by using deep reactive ion etching (DRIE). Reduction of the parasitic capacitance to the substrate is achieved using reverse-biased pn junction diodes. A parasitic capacitance of 0.05 pF has been demonstrated by this approach. This three-dimensional architecture allows for elegant wafer-level packaging through simple flip-chip bonding of the chip's backside to a printed circuit board (PCB) or a signal processing circuit.

What is claimed is:

1. A wafer having front side and back side surfaces and through wafer interconnects characterized in that said interconnects comprise:

a plurality of spaced vias extending between the front side and back side surfaces of said wafer;

a conductor within said vias extending to said front side and back side surfaces; and

conductive pads on the front side and back side surfaces in electrical contact with the ends of said conductor, said front and back side surfaces comprising an n-type or p-type material forming a pn junction between said pads and said wafer whereby to form depletion regions in said wafer opposite the pads and means for applying reverse bias to the said pn junction to increase the width of the said depletion region.

2. A wafer as in claim **1** in which said conductor vias comprises n-type or p-type material forming a pn junction between said conductor and said wafer whereby to form depletion regions in said wafer opposite said conductor and means for applying a reverse bias to the said pn junction to increase the width of the said depletion region.

3. A wafer as in claim **1** or **2** in which the conductor and pads are metal and form a Schottky junction with the wafer and increase the width of the said depletion region by applying a reverse bias to the said Schottky junction.

4. A wafer as in claims **1** or **2** in which the conductor and pads form an MIS junction with wafer.

5. A two-dimensional device array comprising:

a plurality of devices formed on the front side of a wafer;

a plurality of spaced vias at least one for each of said devices extending between the front side and back side surfaces of said wafer;

a conductor within said vias extending between said front side and back side surfaces;

a conductive pad for each of said devices on the front side of said wafer and in electrical contact with the conductor, said conductive pad comprising an n-type or p-type material forming a pn junction with said wafer to form a depletion region in said wafer opposite said pad and means for applying a reverse bias to the said pn junction to increase the width of the said depletion region; and

a conductive pad on the back side of said wafer in electrical contact with the conductor, said conductive pad comprising n-type or p-type material forming a pn junction with the wafer to form a depletion region in said wafer opposite to the pads and means for applying a reverse bias to the said pn junction to increase the width of the said depletion region.

6. A two-dimensional device array as in claim **5** in which said via conductor comprises n-type or p-type material forming a pn junction between said conductor and said wafer whereby to form depletion regions in said wafer opposite said conductor and means for applying a reverse bias to the said pn junction to increase the width of the said depletion region.

7. A two-dimensional device array as in claim **5** or **6** in which the pads and conductor are metal which form a Schottky junction with the wafer and means for applying a reverse bias to the said Schottky junction to increase the width of the said depletion region.

8. A two-dimensional device array comprising:

a plurality of devices formed on the front side of a wafer;

a plurality of spaced vias at least one for each of said devices extending between the front side and back side surfaces of said wafer;

a conductor within said vias extending between said front side and back side surfaces; and

a conductive pad for each of said devices on the front side of said wafer and in electrical contact with the conductor, said conductor and conductive pad isolated from the wafer by a rectifying junction and means for applying a reverse bias voltage across said junction to form a wide depletion region and decrease the parasitic capacitance between said conductor and pads and the wafer.

9. A two-dimensional array as in claim **8** in which the junction is a pn junction.

10. A two-dimensional array as in claim **8** in which the junction is an MIS junction.

11. A two-dimensional array as in claim **8** in which the junction is a Schottky junction.

12. A two-dimensional array as in claim 8 in which the junction between the pads and wafer is a pn junction and the junction between the conductor and wafer is an MIS junction.

13. A wafer having front side and back side surfaces and through wafer interconnects characterized in that said interconnects comprise:

a plurality of spaced bias extending between the front side and back side surfaces of said wafer;

a conductor within said bias extending to said front side and back side surfaces; and conductive pads on the front side and back side surfaces in electrical contact with the ends of said conductor,

means forming a junction between said conductor and pads and said wafer to form a depletion region; and

wherein the depletion region can be increased by the application of a reverse bias voltage to said junctions.

14. A wafer as in claim 13 wherein the junction is a Schottky junction.

15. A wafer as in claim 13 wherein the junction is an MIS junction.

16. A wafer as in claim any one of 13, 14 and 15 including means for applying a reverse bias voltage to said junction to increase the width of the depletion region.

17. An array of ultrasonic transducer devices comprising:

a plurality of devices formed on the front side of a wafer;

a plurality of spaced vias at least one for each of said devices extending between the front side and back side surfaces of said wafer;

a conductor within said vias extending between said front side and back side surfaces;

a junction between said conductor and said wafer to form a depletion region between said conductor and wafer;

a conductive pad for each of said devices on the front side of said wafer and in electrical contact with the conductor,

a junction between said conductive pad and said wafer to form a depletion region in said wafer opposite said pad;

a conductive pad on the back side of said wafer in electrical contact with the conductor; and

a junction between said conductive pad and said wafer to form a depletion region in said wafer opposite to the pads.

18. A wafer as in claim 17 wherein the junction is a Schottky junction.

19. A wafer as in claim 17 wherein the junction is an MIS junction.

20. A wafer as in claims any one of 17, 18 and 19 including means for applying a reverse bias voltage to said junction to increase the width of the depletion region.

* * * * *

AN EFFICIENT ELECTRICAL ADDRESSING METHOD USING THROUGH-WAFER VIAS FOR TWO-DIMENSIONAL ULTRASONIC ARRAYS

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Abstract - This paper presents a technology for high density and low parasitic capacitance electrical interconnects to arrays of Capacitive Micromachined Ultrasonic Transducers (CMUTs) on a silicon chip. Vertical wafer feedthroughs (vias) connect an array of sensors or actuators from the front side (transducer side) to the backside (packaging side) of the chip. A 20 to 1 high aspect ratio 20 μm diameter via is achieved by using Deep Reactive Ion Etching (DRIE). Reduction of the parasitic capacitance of the polysilicon pads to the substrate can be achieved by using Metal Insulator Semiconductor (MIS) operating in the depletion region. This three-dimensional architecture allows for elegant packaging through simple flip-chip bonding of the chip's back side to a printed circuit board (PCB) or a signal processing chip.

I. INTRODUCTION

One of the main problems in fabricating two dimensional ultrasonic transducer arrays is the addressing of the individual array element [1][2][3]. If the array size is large, a significant sacrifice in the array element area is required if the addressing is done through a routing network. Although ultrasonic transducers are considered here, this problem is a challenge for any kind of array fabrication. This paper presents a solution with technology that provides electrical contacts to arrays of MEMS devices on a silicon chip.

The architecture is based on through-wafer vertical vias with high aspect ratio. Many processes have been previously used to fabricate through-wafer interconnects [4][5] including dry etched polysilicon filled interconnects by Chow et al [6]. This work integrates similar interconnects into an active sensor array and makes improvements in achievable capacitance. Compared with our previous two-dimensional array work [2], this interconnects technology demostrated lower parasitic capacitance with ease in doing standard photolithography instead of using dry film photoresist. Bringing the contacts to the backside of the wafer allows for efficient, elegant, and compact packaging through flip-chip bonding to a PCB or signal processing chip. The front side of the wafer can be dedicated solely to the active devices, maximizing their efficiency, whereas the backside contains the flip-chip connection. In this way we have been able to fabricate a 128 x 128 array with an array element size of 420 μm x 420 μm. Reduction of both the parasitic capacitance and leakage current of the pads on both sides and the through-wafer via is the main issue in optimizing the fabrication process. The optimum solution for these interconnects is reverse-biased pn-junction diodes on the front and back sides of the wafer, and a reverse-biased Metal Insulator Semiconductor (MIS) junction inside the via. In this way, it is possible to reduce the parasitic capacitance into the sub-picofarad range. An alternative solution is used in this paper by applying MIS on both pads and vias. The front side of the wafer is fully populated with the ultrasonic array elements, where the backside contains only a small pad for flip-chip bonding.

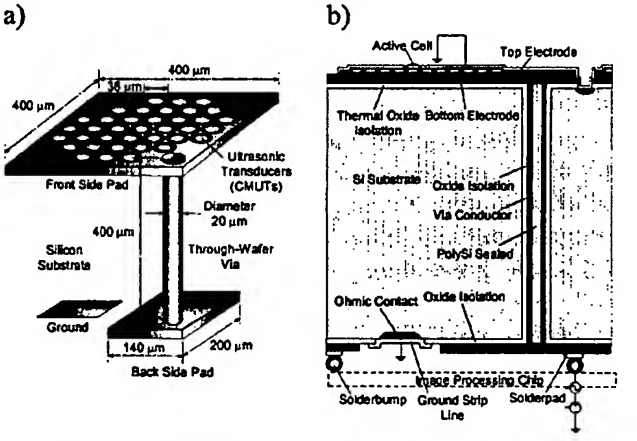

Figure 1. a) MIS through wafer via schematics
b) MIS through wafer via cross section.

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II. DEVICE CONSIDERATIONS

Parasitic capacitance has a detrimental effect on the performance of the CMUT. As shown in Figure 1a, the parasitic capacitance comes about from the 400 μm x 400 μm front side pad, the 200μm x 140μm back side pad, and the 20 μm diameter by 400 μm long through-wafer via that connects the two pads. The front side pad contributes most of the parasitic capacitance. For an MIS device, the capacitance is decreased by operating the device in the depletion region at high frequency. A very low doping concentration substrate is used to increase the depletion depth that results in a decrease of the capacitance (Fig. 1b). To further reduce the parasitic capacitance, a pn junction front side pad will be used that will be discussed in the paragraph of future work.

III. Through-Wafer Via Process

The process flow is shown in Fig. 2. We start with a 400 μm thick double-sided polished n-type <100> Si wafer which is thermally oxidized to 2 μm thick to serve as a hard mask for the deep etch. Both sides are then patterned with 20 μm diameter openings for each via. The through-wafer deep etch is done by etching half way from both sides of the wafer (Fig. 2a). By this means, a 20 to 1 high aspect ration via hole can be achieved. When the via is etched through, the helium flow used for cooling goes through the etched holes, and the etching will be slowed down, serving as an etch stop. The oxide mask is then removed by buffered oxide etch (BOE). For MIS isolation, via side walls and wafer front and backside pads are grown with 1 μm of thermal oxide (Fig. 2b). A layer of 2 μm polysilicon is deposited and then heavily doped with phosphorous to enhance the conductance (Fig. 2c). A layer of low temperature oxide (LTO) is deposited to serve as an etching stop for the etch-back of polysilicon deposited in the following step. The via holes are then filled with polysilicon (Fig. 2d). The polysilicon on both sides is then etched back and stopped on the LTO (Fig. 2e). After removing the LTO, the 2 μm doped polysilicon is exposed again and ready to be etched for the front and back side pads patterning (Fig. 2f). The oxide is opened on the back side for ground opening and heavily doped for ohmic contact The SEM pictures show the cross section of a finished via in Fig. 3. After this step, the ultrasonic transducers (CMUTs) can be built on top of the front side polysilicon (Fig. 4). At the very end, the back side metal pads for flip-chip bonding are formed by lift-off. The wafer is ready for flip-chip bonding to a circuit chip or PCB.

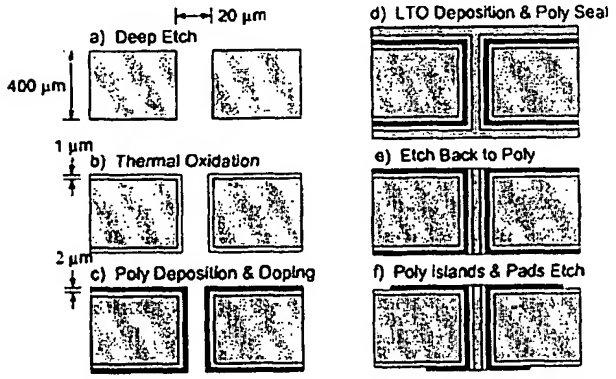

Figure 2. Fabrication Process for a through-wafer via.

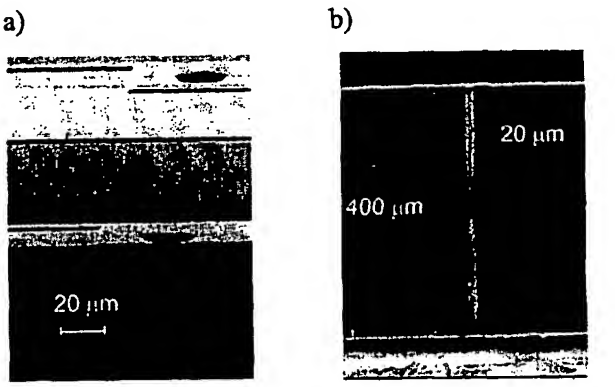

Figure 3. SEM picture of the cross section of the via.

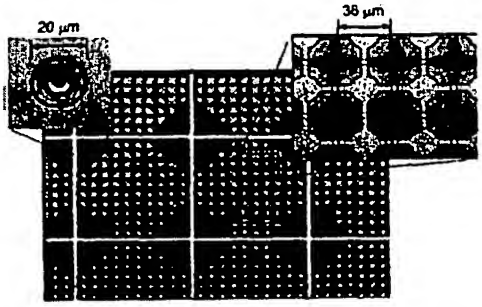

Figure 4. Photograph of the transducers with vias.

IV. TESTING RESULTS

I-V Characterization of Continuity for Through-Wafer Vias with MIS Pads

A testing device with two through-wafer vias connected with a pad on the front side and two pads on the backside is employed to obtain I-V characteristics of the via continuity.

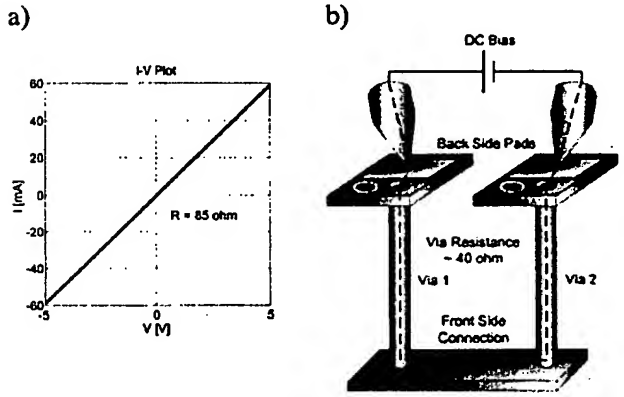

Figure 5. Electrical continuity test set-up.

As shown in Fig. 5, this is a pure resistor with a resistance of 85 Ω. The resistance of one via is thus around 40 Ω, which is satisfactory for the ultrasonic transducer application.

I-V Characterization of Isolation for Through-Wafer Vias with MIS Pads

A testing device with two through-wafer vias isolated with a layer of thermal oxide grown on the silicon substrate is employed to obtain I-V characteristics of the via isolation.

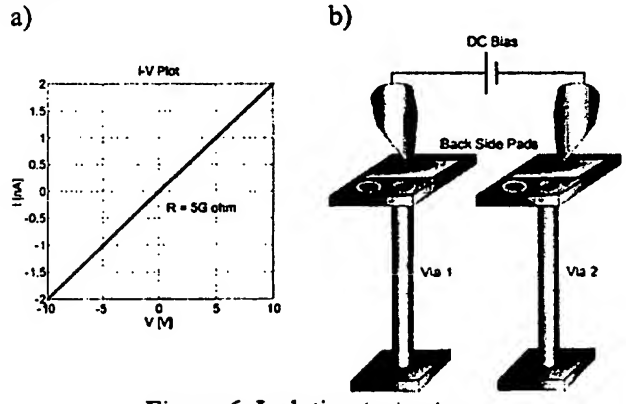

Figure 6. Isolation test set-up.

As shown in Figure 6, the leakage current at 10 volts is only 2 nA and the resistance is 5 GΩ. This means via isolation is sufficient for our application.

C-V Characterization of Through-Wafer Vias with MIS Pads

A testing device with a through-wafer via connected with both front side and back side pads and a ground to the substrate is employed to measure the C-V characteristic. The total capacitance is the capacitance of the via plus both pads.

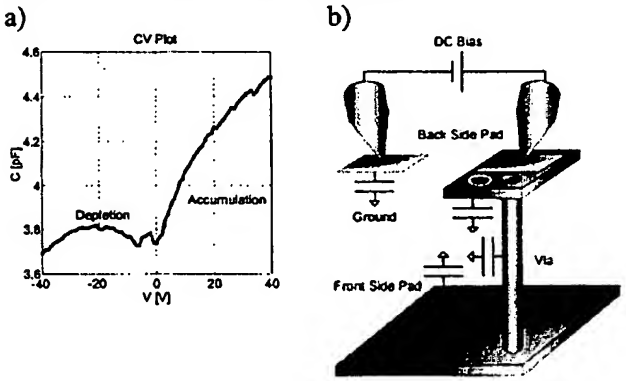

Figure 7. Capacitance measurement set-up.

Figure 7 shows a MIS C-V characteristics at 1 MHz frequency. By applying a reverse bias, the capacitance will decrease because of depletion into the substrate.

Impedance Measurement of CMUTs with Vias with MIS Pads

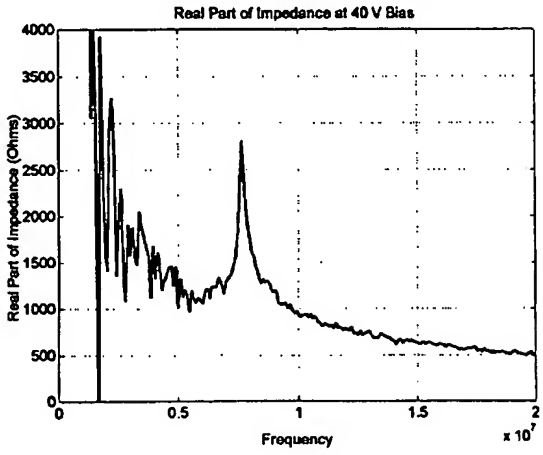

Figure 8. Impedance of CMUTs with Vias.

The experimental setup is similar to that of the CV measurement but with integrated CMUTs on the front side pad. Figure 8 shows the input impedance of a CMUT array element connected to the wafer back side with a via operating at 40 volts applied bias. The resonance frequency is at 7.5 MHz. We obtained a 3.76 pF total capacitance which corresponds to a 2.76 pF parasitic capacitance by subtracting the 1 pF capacitance of the CMUT.

V. FUTURE WORK

Most of the parasidic capacitance is contributed by the front side 400 μm x 400 μm pad. In order to reduce the parasitic capacitance, the front side and back side pads need to be depleted to the substrate by using pn junction devices. As shown in Fig. 8, there are oxide openings on both sides for the pn junction devices. Simulation predicts the total parasitic capacitance can be reduced to 1.5 pF.

Figure 8

VI. CONCLUSIONS

A two-dimensional ultrasonic transducer array with through-wafer vias have been achieved. According to the testing results, the ultrasonic transducers with vias work at our designed frequency 7.5 MHz with an achieved a parasitic capacitance of 2.76 pF. Currently we are optimizing device performance by improving the transducer design and integrating PN junctions under the pads.

VII. ACKNOWLEDGEMENT

This work is sponsored by the Office of Naval Research.

VIII. REFERENCES

[1] B. T. Khuri-Yakub, C. H. Cheng, F. L. Degertekin, S. Ergun, S. Hansen, X. C. Jin, and O. Oralkan, "Silicon Micromachined Ultrasonic Transducers," presented at the Fifth European Conference on Underwater Acoustics, Lyon France (July 10-13, 2000).

[2] S. Calmes, C. H. Cheng, F. L. Degertekin, X. C. Jin, and B. T. Khuri-Yakub, "Highly Integrated 2-D Capacitive Micromachined Ultrasound Transducers," presented at the 1999 IEEE International Ultrasonics Symposium, Lake Tahoe, Nevada; in Ultrasonics Symposium Proceedings, pp. 1163-6. (Octobor 17-20, 1999)

[3] X. C. Jin, C. H. Cheng. O. Oralkan, S. Calmes, F. L. Degertekin, and B. T. Khuri-Yakub, "Recent Progress in Capacitive Micromachined Ultrasonic Immersion Transducer Array," presented at the 8th International Symposium on Integrated Circuits, Devices and Systems, Singapore; in ISIC-99 Proceedings, pp.159-162. (September 8-10, 1999)

[4] H. T. Soh, C. P. Yue, A. McCarthy, et al., "Ultra-low resistance, through-wafer via (TWV) technology and its application in three dimensional structures on silicon", Japanese Journal of Applied Physics, Part I 38(4B) 2393-6 (1999)

[5] T. R. Anthony, "Forming electrical interconnections through semiconductor wafers", Journal of Applied Physics, 52(8) 5340-9 (1981).

[6] E. M. Chow, A. Partridge, C. F. Quate, T. W. Kenny, "Through-Wafer Electrical Interconnects Compatible with Stanford Semiconductor Processing", Solid-State Sensor and Actuator Workshop, Hilton Head Island, South Carolina, June 4-8, 2000, pp. 343-6 (2000)

Process Compatible Polysilicon-Based Electrical Through-Wafer Interconnects in Silicon Substrates

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***Abstract*—Electrical through-wafer interconnects (ETWI) which connect devices between both sides of a substrate are critical components for microelectromechanical systems (MEMS) and integrated circuits (IC), as they enable three-dimensional (3-D) structures and permit new packaging and integration geometries. Previously demonstrated ETWI are very difficult to integrate with standard semiconductor fabrication processes, not compatible with released sensors, do not permit extensive processing on both sides of the wafer, and are in general very application specific. This work describes the design, fabrication, and characterization of an ETWI technology for silicon substrates that can be broadly integrated with MEMS and IC processes. This interconnect is a passively isolated electrical through-wafer polysilicon plug, with a 20 μm diameter, 10–14 Ω resistance, and less than 1 pF capacitance. Plasma etching from both sides of the wafer is used to achieve a high-aspect ratio via (20 : 1 through 400 μm). The process is compatible with standard lithography, standard wafer handling, subsequent high-temperature processing, and released sensors integration. N-type and p-type versions are demonstrated, and isolated ground planes are added to provide shielding against substrate noise. Electrical properties of these ETWI are measured and analytically modeled. These ETWI are appropriate for integration with devices with impedances much greater than the ETWI, such as piezoresistive and capacitive sensor arrays. [850]**

***Index Terms*—Electrical through-wafer interconnects (ETWI), MEMS and IC integration, through-wafer via deep silicon plasma etch.**

I. Introduction

SEMICONDUCTOR device fabrication is predominantly based on planar fabrication processes, with devices on only one side of a substrate. Bulk micromachined devices can involve three-dimensional (3-D) structures, sometimes even through the entire substrate, but devices are rarely electrically connected through the substrate. The trend toward more complicated systems involving chips from incompatible fabrication technologies has led to increased pressure for 3-D electrical interconnect and packaging technologies. Currently there are a variety of ways to compactly connect multiple chips, using peripheral wiring technologies, such as wire-bonding, tab connectors, or flex circuits. For the highest interconnection density, however, area interconnections with electrical through-wafer interconnects (ETWI), as opposed to peripheral interconnects, are required [1], [2].

ETWI are being pursued for a variety of integrated circuits applications. ETWI could provide ground and power between chips in a stack or for a single chip to its package. A low impedance substrate via connection to a backside common ground is an important way to reduce parasitics in RF circuits, and has been demonstrated in both silicon and gallium arsenide substrates [3]–[5]. Such a ground connection can also be used to protect sensitive analog sections of a mixed signal chip from noisy digital circuits with a Faraday cage [3]. Multiple ETWI have been connected with patterned metal lines to form a 3-D coil inductor through a substrate [6]. When combined with wafer bonding or flip chip technology, stacks of multiple memory chips are possible [7], [8]. While ETWI with diameters between 30 μm and 150 μm were sufficient for these applications, smaller diameters (<10 μm) are required for 3D circuits, where the motivation is to shorten metal line lengths of a single circuit design [9].

In the area of micro-electro-mechanical-systems (MEMS), ETWI also have significant applications. MEMS sensors generally interact with the environment, which may or may not be compatible with electrical connections and standard IC chip packages. For devices that require close proximity to a sample, such as proximal probe sensors, sensor-side wire bonds that are hundreds of microns tall dramatically restrict available sensing geometry. In the case of 2-D arrays of scanning probe cantilevers, which need to be within a few microns of the sample or closer, this restricts the sample size to the size of the chip. Cantilever arrays have been integrated with ETWI in both silicon [10]–[13] and glass substrates [14]. For sensors that interact with a corrosive or electrically conducting environment, ETWI effectively protect the electrical signals without having to embed wire-bonds in protective adhesives. Applications include underwater proximity sensing arrays and cantilever sensors for biochemical applications [15]–[18]. For sensor arrays that need to be high-density, such as for focal plane arrays, ETWI serve to move electrical wiring away from the sensor side to allow for higher fill factors. Vertical chip stacking, enabled by ETWI, are an attractive way to integrate IC and MEMS, as they allow optimized incompatible processes to be combined with bonding.

ETWI fabrication technology can be classified by its through-substrate etching technology (see Fig. 1). Though

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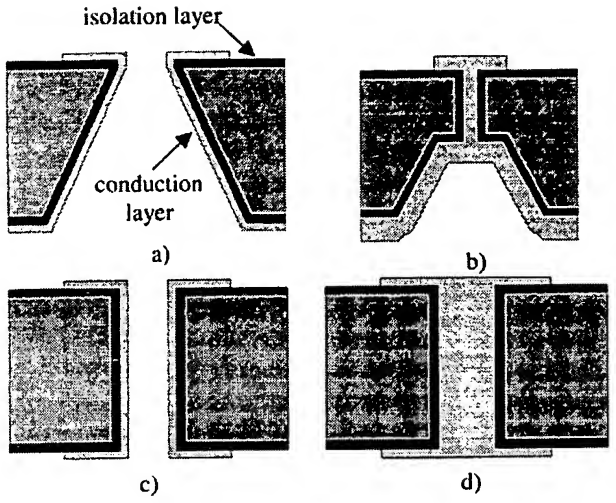


Fig. 1. Schematic of various ETWI fabrication technologies based on (a) wet anisotropic etching alone, (b) wet and plasma anisotopric etching, (c) plasma anisotropic etching alone, and (d) plasma anisotropic etching with filling. Only option (d) permits double-sided standard spin-on lithography and maximizes packing density on both sides of the wafer.

ETWI are being pursued in other materials such as glass and gallium arsenide [4], [19]–[23], this work focuses on silicon. To not limit packing density, the ETWI via diameters should be smaller than the connecting devices. Wet processing can be used for bulk etching through a silicon substrate, but this restricts via sizes to over 100 μm diameters for standard wafer thicknesses (>400 μm). Electrical wiring densities can be increased by developing sidewall lithography techniques, but this requires electrodeposited photoresist or shadow masking [24]–[26]. Recently, isotropic silicon plasma etching has been used to form ETWI in silicon [27]. The vias are large (200 μm), but for wafer stacking applications, this work achieves an important task, which is to expose an isolated connection on the backside of the wafer for bonding without needing to perform backside lithography. Anisotropic etching can be combined with isotropic etching to form smaller vias (~10 μm diameters), but wiring density is still limited by the large via [3], [28]. Anisotropic etching alone achieves smaller vias on both sides of the wafer, as 30 μm diameters through a 500 μm wafer have been demonstrated using plasma etching [6], [29]. After depositing the conduction layer, however, the vias were not filled so electroplated resist was required for lithography. Wafer thinning can be used to reduce aspect ratios, making etching, and thin-film deposition easier [30]. However, thin wafers are often too delicate to handle in standard semiconductor processing equipment, thus requiring a carrier wafer which hinders processing on both sides of the wafer.

This work presents a preprocess, full-wafer thickness approach that is compatible with standard semiconductor processing. Conventional IC and MEMS lithography, thin-film deposition and thin-film etching processing can be subsequently performed. The ETWI are high density (20 μm diameters) and filled with doped polysilicon to permit standard spin-on photoresist lithography on both sides of the wafer. In contrast to the above post-process work based on metal deposition, subsequent high-temperature steps such as thermal oxidations (>1000 °C) are permitted. When ultra low resistance (<1 Ω) is required, such as for RF applications, copper and other metals might be required, making the pre-process approach inappropriate. However, when slightly larger impedances are satisfactory, the pre-process ETWI is attractive because integration requires minimal changes to the original device process. In addition, the "pre-process" ETWI permits high-temperature (>500 °C) chemical vapor deposition techniques, which simplifies high aspect ratio via filling. For integration with delicate free-standing MEMS sensors, such as cantilevers and membranes, ETWI fabrication prior to device fabrication is preferred. Our initial work presenting a tungsten [10]–[12] and n-type polysilicon based ETWI [31] is expanded here to include p-type and shielded ETWI. P-type ETWI facilitate integration with p-type piezoresistive sensors, and integrated shielding reduces substrate noise coupling to the ETWI. The design, fabrication and characterization of these devices are presented.

II. Design

The ETWI were designed for integration with 2-D arrays of released MEMS sensors. While the specific requirements for an ETWI vary with the application, the design presented here is appropriate for piezoresistive cantilever arrays [10], [11], ultrasound transducer arrays [15], and proximity sensor arrays [18], [32]. For these devices, an ETWI with less than 100 Ω resistance, 1 pF capacitance and 30 μm diameter footprint is satisfactory because the impedance of the sensor is orders of magnitude greater than the ETWI. Fig. 2 depicts theoretical resistance values for ETWI in 400 μm thick substrates for cylindrical vias using only high-temperature compatible materials. The heavily doped polysilicon ETWI assume the full radius of the via is conducting, while the tungsten ETWI assumes a one micron conduction layer, as material stress prohibits thicker films. The tungsten could be followed by polysilicon deposition to fill the via, but this process is not permitted in our lab. Substrate coupling capacitance values are calculated for thick thermally grown silicon dioxide and deposited silicon nitride (see Fig. 2). Active isolation, such as with reverse biased diodes is also possible, but passive isolation is simpler to integrate and the focus here [33], [34]. Thicker oxide films are possible using sacrificial polysilicon oxidation and adding a nitride reduces the capacitance by 30% compared to that of oxide alone, but both add etching complexity. These films are deposited with high temperature chemical vapor deposition (500–1000 °C) and have very low sticking coefficients, so they have excellent deposition conformity in high-aspect ratio vias. A via with a radius of 5–20 μm satisfies our electrical requirements, but the current limits on achievable etch depth and aspect ratio limit our via radius to 10 μm through a 400 μm silicon substrate. Thus the design selected was a 10 μm radius via, with 2 μm thermal oxide isolation, and heavily doped polysilicon conduction. This gives a predicted minimum resistance of 5 Ω (n-type) and 25 Ω (p-type) and a capacitance of 0.5 pF.

An ETWI shielded with a driven ground plane can protect ETWI signals from substrate noise, reduce cross-talk between ETWI, and enable higher ETWI packing density. Piezoresistive

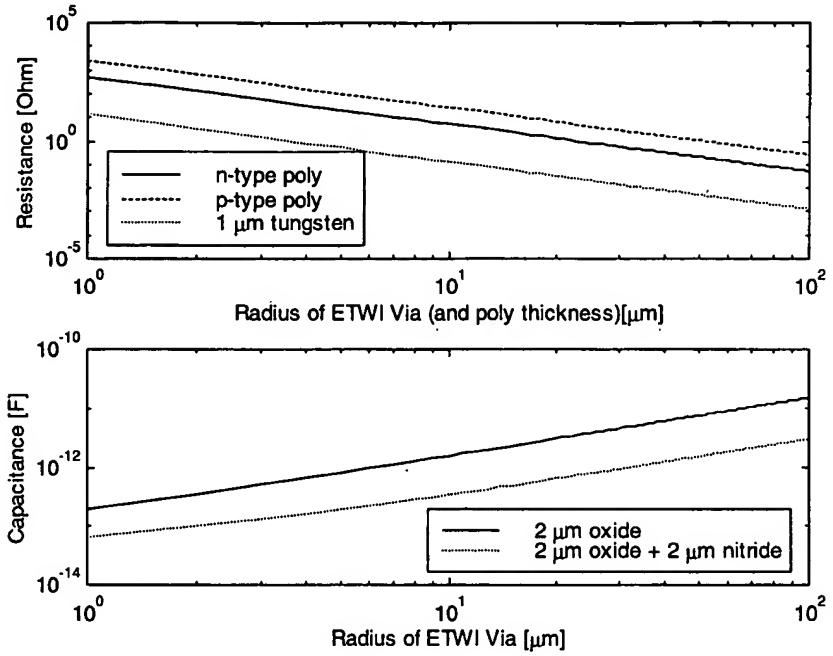


Fig. 2. Theoretical minimum resistance and capacitance for preprocess cylindrical ETWI for a 400 μm thick silicon substrate.

sensors generate small voltage signals (μV range) that are vulnerable to external noise, especially before amplification. Potential noise sources include high voltage actuators or integrated circuits [35], [36]. The polysilicon ETWI designed in the previous section can be integrated with a conductive polysilicon ground shield surrounding the ETWI [see Fig. 3(a)]. Thermal oxide can be used on both sides of the ground shield for isolation between the substrate and the signal ETWI core. A shield of 1 μm thick polysilicon that is heavily doped n-type to achieve a minimum resistivity of 400 $\mu\Omega$-cm has a theoretical resistance of 60 Ω. The actual resistance to the driven ground pad is larger because of the connections on the surface and the bond pad, suggesting a conservative shield to ground resistance of $\sim$100 Ω. For 1-μm-thick thermal oxide the capacitance is 1 pF, approximately double the capacitance between the shield to signal ETWI (C_{etwi}). This shielded ETWI is targeted for piezoresistive cantilever applications that operate at frequencies less than 100 kHz. For these frequencies, the signals have wavelengths significantly larger than the dimensions of the devices, suggesting that a lumped RC model is adequate for modeling. A substrate signal, in this approximation, would see AC circuit paths to ground through the shield and then through the ETWI [see Fig. 3(b)].

Solving this circuit for the ratio of $V_{\text{etwi}}/V_{\text{sub}}$ gives

$$\frac{V_{\text{etwi}}}{V_{\text{sub}}} = Z_1 Z_2 = \left(\frac{R_{\text{shield}}}{R_{\text{shield}} + Z_{C_{\text{shield}}}}\right) \cdot \left(\frac{\frac{1}{2}R_{\text{etwi}}}{R_{\text{shield}} \| Z_{C_{\text{shield}}} + Z_{C_{\text{ETWI}}} + \frac{1}{2}R_{\text{etwi}}}\right) \quad (1)$$

where V_{sub} is the substrate voltage, C_{shield} the shield oxide capacitance ($Z_{C_{\text{shield}}}$ its impedance), R_{shield} the shield resistance, C_{etwi} the ETWI oxide capacitance to the shield, V_{etwi} the voltage on the ETWI, and R_{etwi} the resistance of the ETWI chain. The symbol "$\|$" is shorthand for impedances in parallel, and R_{etwi} is in parallel with a matching resistor in a bridge circuit. For the case of no shield, (1) can be used to calculate the coupling assuming R_{shield} and C_{shield} go to infinity. The effectiveness of the shield can then be characterized as the difference between the coupling when the shield is on and the coupling when the shield is not present. Using, $R_{\text{etwi}} = 5\ \Omega$, $C_{\text{etwi}} = 0.5$ pF, $R_{\text{shield}} = 100\ \Omega$, and $C_{\text{shield}} = 1$ pF, (1) predicts that the shield will provide 100 dB of relative shielding at 10 kHz (see Fig. 4).

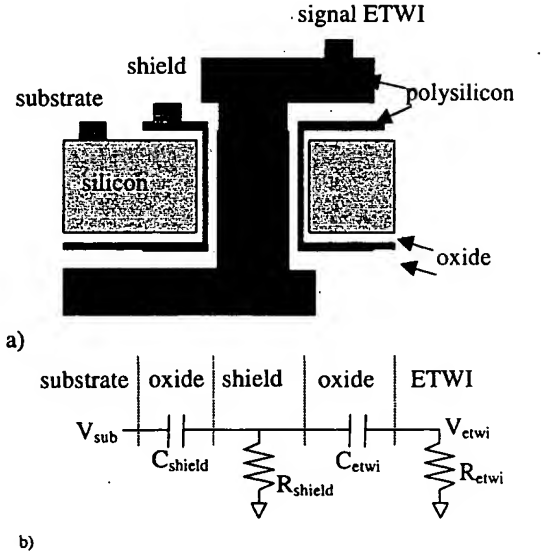


Fig. 3. (a) Schematic of an ETWI with an isolated ground shield and (b) a lumped circuit model.

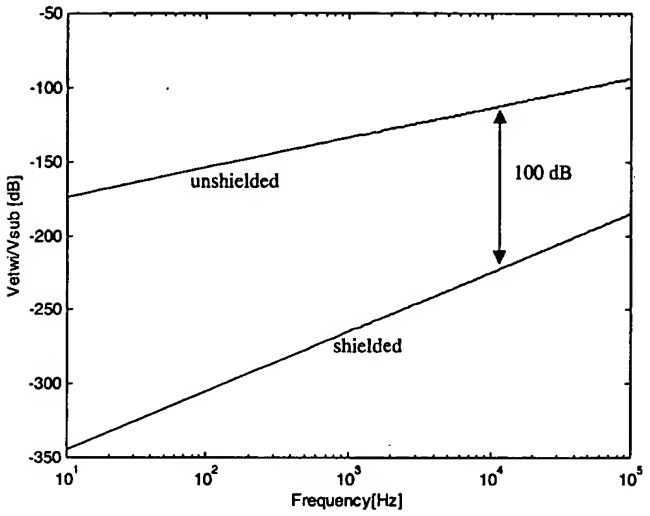


Fig. 4. Theoretical substrate noise coupling to one ETWI with and without a ground shield.

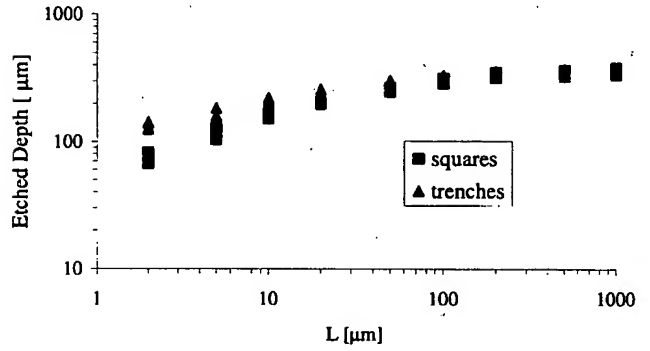


Fig. 5. Etch depth for squares of side length L and trenches of dimensions $L \times 1000$ μm. The following etch recipe was run for 80 min: SF_6 flow rate 130 sccm, SF_6 active time 11 s, etch electrode power 12 W, C_4F_8 flow rate 85 sccm, C_4F_8 active time 8 sec, passivation electrode power 0 W, coil power 600 W, APC angle 70° (pressure control).

III. Fabrication

Our previous work described the fabrication process for a polysilicon filled ETWI without a ground shield [31]. Here we present the process for a shielded ETWI, which includes the steps for an unshielded version. A key initial step is to use high-density plasma etching based on time multiplexed etching (SF_6) and passivation (C_4F_8) to form a 20 μm diameter via through a 400 μm thick silicon wafer [37]. Etches with the required aspect ratios (>20 : 1) have been previously reported, but they are of trenches, with one dimension very long (>1000 μm), or not deep enough to go through a 400-μm-thick wafer [30], [38], [39]. Aspect ratio dependent etching, where smaller areas etch slower, is a characteristic of fluorine-based etches [40]. We have observed this effect to be particularly severe when one dimension of the pattern is less than 100 μm (see Fig. 5). By etching from both sides of the wafer, the average etch rate is higher, which shortens the total etch time and permits the use of thinner masks. The required aspect ratio is reduced by a factor of two to 10 : 1. Standard 10 μm photoresist masks are initially patterned on both sides of the wafer and aligned to each other.

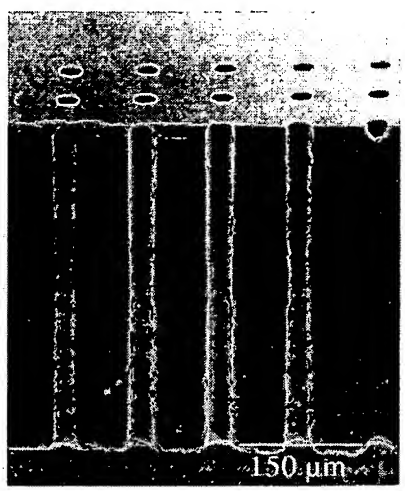


Fig. 6. Cross-section scanning electron microscope (SEM) image of a 20-μm diameter via through a 400-μm-thick silicon wafer formed using plasma etching.

The etch is performed for 150 min from topside and then approximately 150 min from the backside (see Fig. 6). It is possible that dual side alignment error could create a slight step at the middle of the wafer. Electrically this could narrow the effective radius and thus increase the resistance, as well as lower breakdown voltages and increase leakage across the dielectric due to increased roughness. The overetch time of the second etch, which punches through, should be minimized to reduce lateral etching of the front side of the silicon. Using an etch recipe with increased passivation for the final 30 min of the etch helps to minimize this effect. The profile of the vias are not perfectly straight and do not have a constant radius, but have an effective radius of 20 μm, as the plasma etch causes a slight taper and thus the radius actually decreases slightly toward the middle of the wafer while mask erosion enlarges the radius at the top and bottom. ETWI with 40 μm pitch have been demonstrated.

After forming the via, conformal thin films are deposited (see Fig. 7). For electrical isolation, wet thermal silicon dioxide (2 μm) is grown at 1100 °C, and for signal conduction, low pressure chemical vapor deposition polysilicon (3 μm) is deposited at 600 °C. To fabricate n-type interconnects, this is followed by phosphorus diffusion at 1000 °C for 30 min from a liquid phosphorus oxychloride ($POCl_3$) source. If p-type interconnects are fabricated, boron diffusion is performed at 1000 °C for 30 min from liquid boron tribromide (BBr_3). The diffusion doping is followed by a buffered hydrofluoric acid (BHF) dip to remove the phosphosilicate glass which forms on wafers during n-type diffusion. For p-type wafers, a borosilicate glass forms during doping which is more difficult to remove, so a BHF dip is followed by 2500 Å wet oxidation at 1000 °C. This converts the glass into an oxide which is then readily removed by another BHF dip. This cycle of polysilicon deposition, doping, and then glass removal, can be repeated to achieve a lower resistance. However, severely overdoping beyond the saturation limit can cause low quality polysilicon layers, forming doping rich phases that etch in BHF and create holes in the polysilicon [41]. For the n-type wafers the doping cycle was repeated twice and for the p-type wafers two or three times. Boron is less conductive

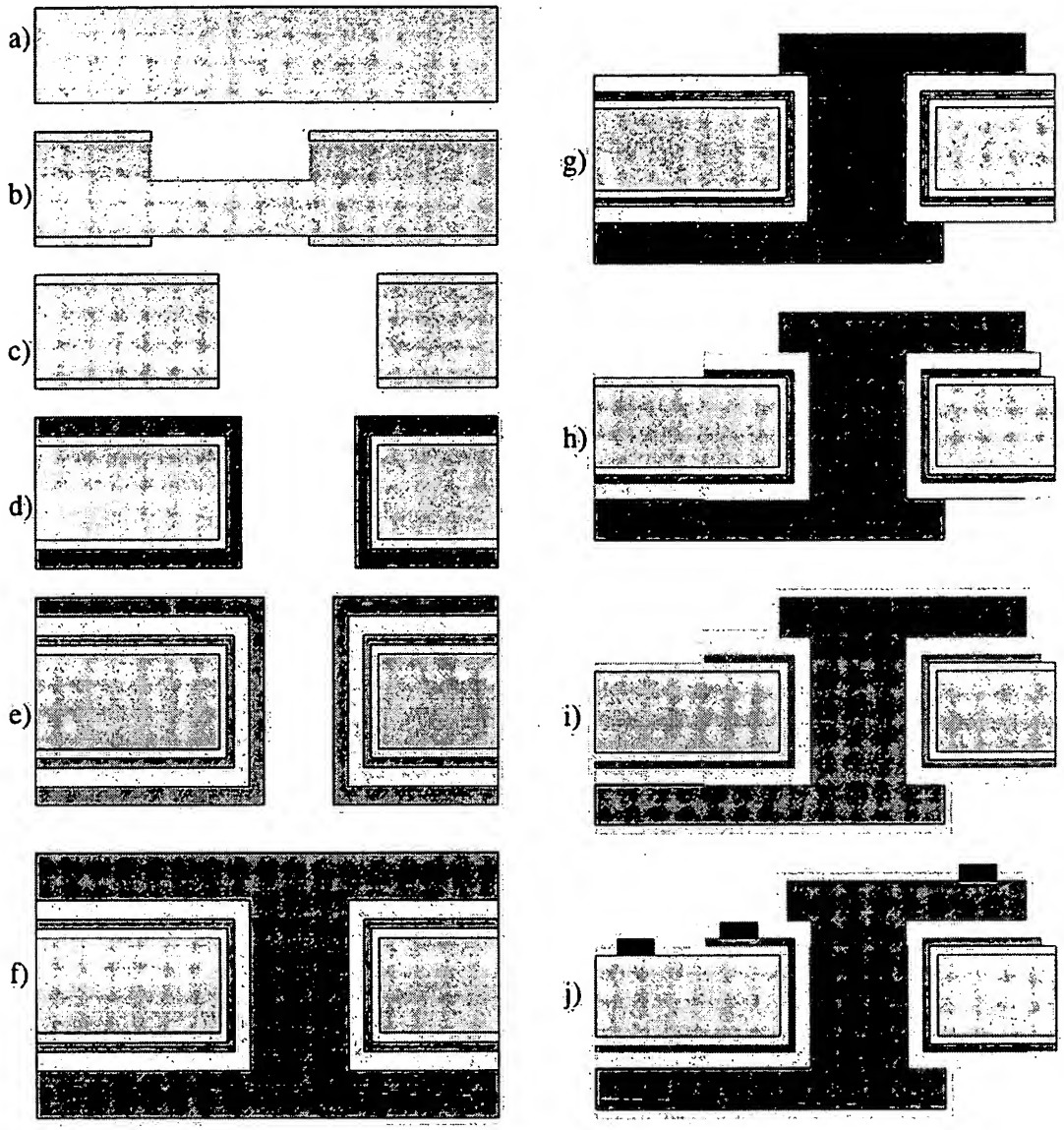
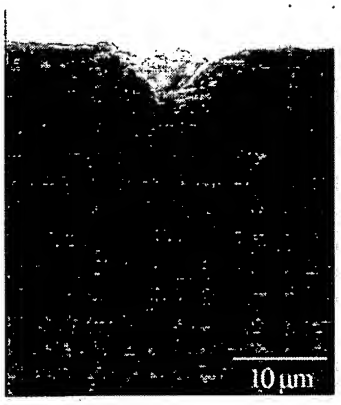


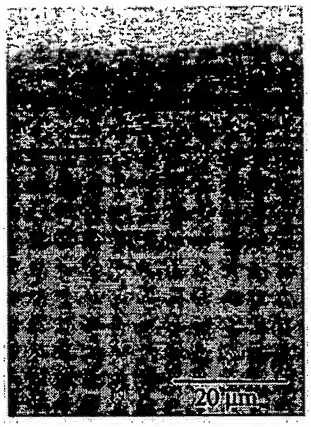
Fig. 7. Fabrication process for a shielded preprocess through-wafer interconnect. (a) Starting silicon substrate. (b) Vias are etched halfway through the wafer with resist masks. (c) The wafer is flipped and holes are etched from the backside of the wafer, meeting the frontside holes. (d) Oxide and then polysilicon are deposited and doped. (e) Oxide and then polysilicon are deposited again for the shield. (f) After diffusion doping, additional polysilicon is deposited to fill. (g) Signal polysilicon is patterned. (h) Shield polysilicon is patterned. (i) Oxide for passivation is deposited and (j) contact vias are etched with a polysilicon mask and metal pads are formed.

than phosphorous so the doping was increased to compensate. To fill the via, more LPCVD polysilicon is deposited (5–7 μm), at 45 min per micron. Shorter filling times might be possible with epitaxial polysilicon, which deposits an order of magnitude faster than LPCVD. Another 30 min phosphorus (or boron) diffusion is performed to make the surface conducting, followed by another BHF dip, and then a 120 –min anneal at 1000 °C to fully drive dopants throughout the polysilicon. This high temperature step, like the others, also serves to relieve stress in the thick polysilicon layers. An occasional ETWI exhibited a polysilicon void in this filling process, but because the ETWI are sealed under vacuum we do not expect subsequent stressing in low-pressure systems. Note the filling process can leave a 3–5 μm dimple at the entrance to the via if insufficient polysilicon is deposited. While one micron photoresist adequately masks over this, planarization techniques such as polishing or etch backs can be used if thinner resist is required for high-resolution optical lithography (see Fig. 8).

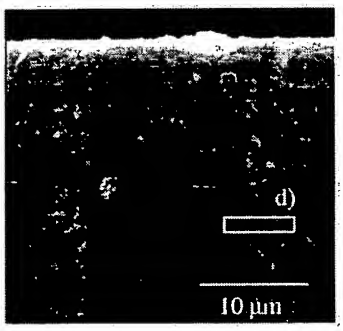
To facilitate ETWI electrical testing, the devices were not polished so the surface layers could be patterned. If no ground shield is required, the top and bottom polysilicon routing are patterned and metal contacts are formed. To add a ground shield, another oxidation must be performed, followed by doped polysilicon deposition [see Fig. 7(e)]. The second thermal oxidation for the shielded case should be the thickest to minimize signal capacitance. If 2 μm are grown, about 1 μm of the underlying polysilicon is consumed. Since dopants diffuse quickly in polysilicon, the anneal and the oxidation drive the



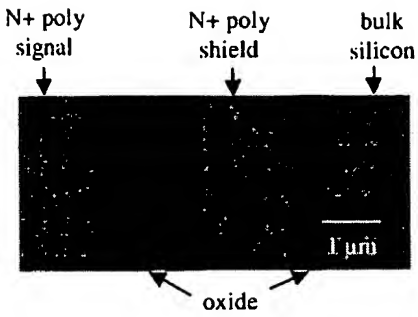
(a)



(b)



(c)



(d)

Fig. 8. Cross-section SEM images of fabricated polysilicon filled ETWI. (a) The top of an ETWI with a dimple, (b) an ETWI with more polysilicon deposition to minimize the dimple, (c) an ETWI after mechanical polishing for planarization, and (d) close up of the layers in a shielded ETWI.

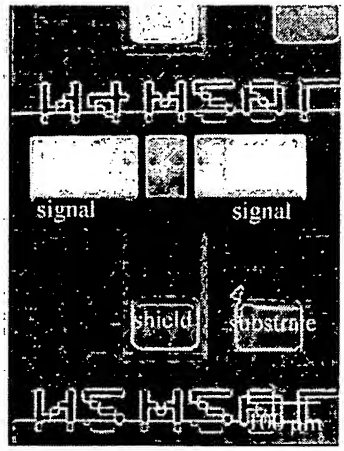


Fig. 9. Scanning electron microscope image of a fabricated shielded ETWI chain with $N_{\mathrm{ETWI}} = 4$.

dopants deeper into the polysilicon, so that a conduction layer still remains after the oxide is grown. The segregation coefficient for phosphorous favors high-doping in the polysilicon, so oxidizing the doped polysilicon can lead to higher phosphorous concentrations and thus a low shield resistance. A standard spin-on photoresist is patterned on both sides, and ETWI chains for characterization are formed [see Fig. 7(g)]. On both sides a 1000 Å polysilicon layer is used as a mask for wet etching the thick isolation oxide, followed by dry etching the polysilicon shield. After 1 μm of low temperature oxide (400 °C) is deposited for passivation, contact windows are opened and sputtered aluminum contacts for wire-bonding are formed (see Fig. 9).

IV. Characterization and Discussion

Chains from 2 to 128 ETWI in series were tested to extract electrical properties of individual ETWI. Ohmic current–voltage relationships were observed for both p-type and n-type ETWI chains. Separate planar test structures were used to measure the resistance of lines connecting each ETWI along the wafer surface. These values were subtracted from the corresponding ETWI chain resistance to yield the resistance of the ETWI chain alone, which when plotted against the number of ETWI in a chain, yields a slope equal to an averaged value of 13 Ω or a single ETWI (see Fig. 10). Four point probe sheet resistance measurements of the doped polysilicon gave 1.1 Ω square, giving a calculated 14 Ω via. The sheet resistance is above the theoretical minimum suggesting that lower resistances could be obtained through increased cycles of doping and annealing. P-type ETWI measured 25 Ω via when two doping and annealing cycles were performed, and reduced to 10 Ω via when an additional cycle was added.

Chains of ETWI and their planar test structures were similarly measured to extract the capacitance of a single ETWI via to the substrate. Because these substrates were not heavily doped (2E14 cm^{-3} to 2E15 cm^{-3} of phosphorous), biasing into depletion adds a series capacitor that lowers the total capacitance, as well as a parasitic series resistance (~300 kΩ). The substrate is grounded and the conducting polysilicon layer voltage is swept,

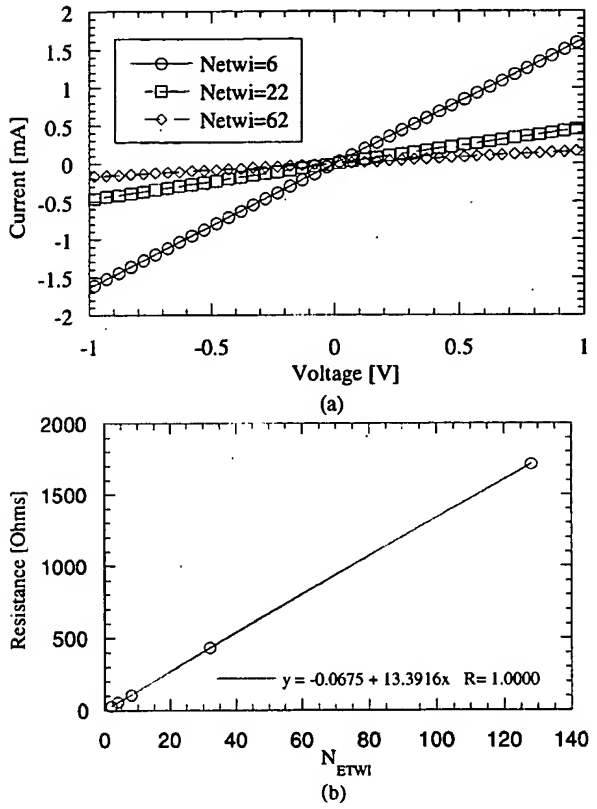


Fig. 10. (a) Ohmic current-voltage curves for p-type chains of different number of ETWI. (b) Resistance as a function of chain length for n-type ETWI after removing planar line resistances. The slope gives an average resistance for a single ETWI resistance of 13 Ω.

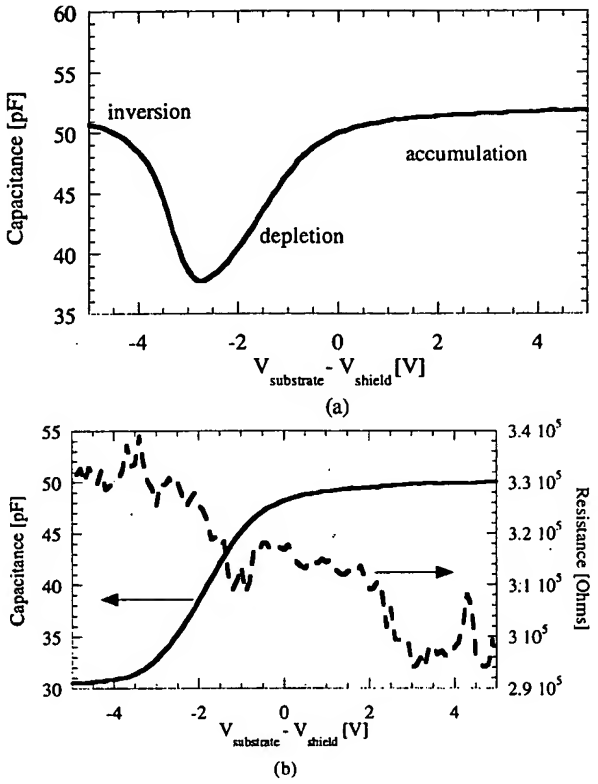


Fig. 11. (a) Low-frequency and (b) high-frequency C–V curves of ETWI oxide between shield and substrate of a shielded ETWI chain of length $N_{\mathrm{ETWI}} = 8$. Test structures with chains of different lengths were measured to extract a capacitance for a single ETWI of 0.6 pF. These are n-type polysilicon ETWI on n-type substrates with 1–20 Ω-cm resistivity.

taking the capacitance through depletion, and then into accumulation, with a flat band voltage of −2.7 V. A typical low and high frequency capacitance–voltage curve is given in Fig. 11, with an oxide capacitance of 52 pF for a chain of 8 ETWI. Planar test structures were also measured to extract the parasitic capacitance due to the planar lines between the ETWI and the bond pads (1 pF). Like the resistance, the oxide capacitance of the ETWI alone were plotted against the number of ETWI. The slope of a fitted line (chi-squared = 0.9999) results in a measured 0.6 pF/via, which matches well with the predicted 0.5 pF/via. For shielded ETWI, the capacitance between the shield and signal was also measured, giving a capacitance of 3.3 pF/via. The shield oxide was 0.6 μm thick, giving a predicted shield capacitance of 2 pF. A source of the increased capacitance is the rough etch caused by the through-wafer etch. The scallops, caused by the switching process the plasma etch, are on the order of 0.5 μm and would be smoothed after the long 2 μm oxidation performed for the nonshielded ETWI. However, for the shielded ETWI, only 0.6 μm was grown, so much of the roughness would remain and result in increased surface area, and thus capacitance.

The effectiveness of the polysilicon shield was characterized by measuring the coupling between the substrate and the ETWI chains. The ETWI were balanced in a Wheatstone bridge circuit and the signal amplified through an instrumentation amplifier to be measured by a spectrum analyzer. Fig. 12 shows how the substrate signal coupling to a chain of 128 ETWI from a 10.7 kHz

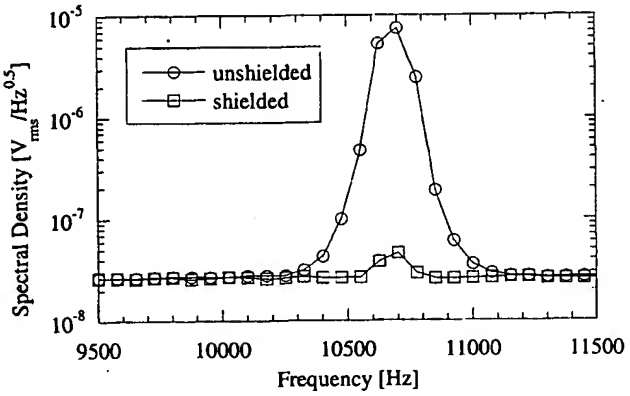


Fig. 12. ETWI signal when substrate driven by 10 kHz, 100 mV for chain of length $N_{\mathrm{ETWI}} = 128$. Shielding reduces the coupling by over two orders of magnitude.

signal applied to the substrate is suppressed by over two orders of magnitude when the shield is driven to ground, relative to the ETWI chain without a shield. The shielding for a single ETWI cannot be directly measured for comparison with the theoretically predicted 100 dB shielding at 10 kHz predicted by (1), as it is difficult to electrically probe both sides of a single ETWI. Shielding measurements for chains of ETWI help to validate the model, but two artifacts from the measurement process, a substrate probe capacitance (C_{probe}) of 0.3 pF and a substrate con-

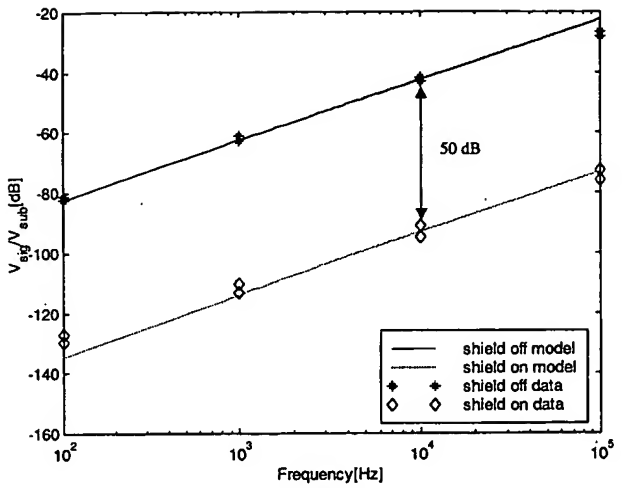


Fig. 13. Absolute magnitude of shielding as a function of frequency for ETWI chain of length $N_{\mathrm{ETWI}} = 128$. The measured data points at each decade are plotted, along with a lumped circuit model, using only measured component values.

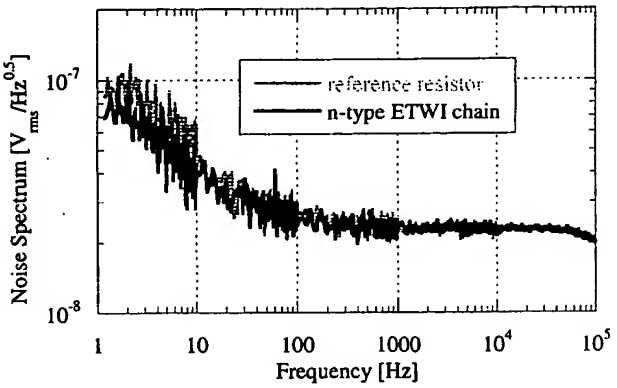


Fig. 14. Noise spectrum for p-type ETWI chain and a metal film reference resistor. The curves are nearly coincident.

tact resistance (R_{sub}) of 300 kΩ (Fig. 11) need to be included, giving,

$$\frac{V_{\mathrm{etwi}}}{V_{\mathrm{sub}}} = Z_1 Z_2 + Z_3 \tag{2}$$

where

$$Z_3 = \frac{Z_{\mathrm{device}}}{Z_{C_{\mathrm{probe}}} + Z_{\mathrm{device}}}$$

$$Z_{\mathrm{device}} = \tfrac{1}{2} R_{\mathrm{etwi}} \| (Z_{C_{\mathrm{etwi}}} + R_{\mathrm{shield}} \| Z_{C_{\mathrm{shield}}})$$

and Z_1 and Z_2 were defined in (1). Because R_{sub} and C_{probe} do not scale with the number of ETWI, they are less significant for longer chains [42]. Measurements identical to Fig. 12 were repeated for each frequency decade between 100 Hz and 100 kHz. The ratio of the shielded and unshielded peak signal in the noise spectrum is plotted as a function of frequency for a chain of length $N_{\mathrm{ETWI}} = 128$ in Fig. 13. Approximately, 50 decibels of shielding are observed over this frequency range. The model parameters consist of only measured component values, $N_{\mathrm{ETWI}} = 128$, $R_{\mathrm{ETWI}} = 2$ kΩ, $C_{\mathrm{ETWI}} = 120$ pF, $R_{\mathrm{shield}} = 100$ Ω, $C_{\mathrm{shield}} = 600$ pF, $R_{\mathrm{sub}} = 300$ kΩ, and $C_{\mathrm{probe}} = 0.3$ pF.

Noise characteristics were measured by placing the ETWI chain in a matched Wheatstone bridge circuit. Devices were wire-bonded into hybrid IC packages to allow complete encapsulation of the device, with exterior shielding to protect from environmental noise. A chain of 128 n-type ETWI was compared to a metal film resistor, both with a resistance of 2000 Ω (see Fig. 14). The ETWI chain and the reference resistor have nearly coincident noise curves. The 1/f noise at 10 Hz is 40 nV/$\sqrt{\mathrm{Hz}}$, which agrees with previously reported results for heavily n-type doped polysilicon resistors [43]. Both measured noise spectra are limited by the electrical system noise floor of 20 nV/$\sqrt{\mathrm{Hz}}$ which exceeds the Johnson noise of a 2000-Ω resistor (5 nV/$\sqrt{\mathrm{Hz}}$) and suggests the ETWI noise are the same or below the reference resistor. P-type ETWI noise curves were also measured to be the same as a metal film reference resistor. While these noise properties are satisfactory for integration with piezoresistive deflection sensors, which are commonly used in released silicon devices, other high-temperature compatible and conformal materials besides polysilicon are also worth investigating for very low $1/f$ noise ETWI applications. Amorphous polysilicon can be grown as large grains, which has the potential to be low noise because reducing the number of grain boundaries is associated with reduced low frequency noise [44], [45]. Similarly, polycrystalline silicon germanium has been shown to have quieter $1/f$ noise characteristics than polysilicon because of reduced barrier potentials [46]. Polycrystalline silicon germanium also has the advantage that it is deposited at a low temperature (<450 °C), so it may have applications in high-aspect ratio post-process ETWI fabrication.

V. Conclusion

An ETWI technology with 10–14 Ω resistance, <1 pF resistance, and 20 μm diameter has been presented using through-wafer plasma etching, thermal oxidation, LPCVD polysilicon deposition, and diffusion doping. The silicon substrate is 400 μm thick, high-temperature compatible, and planar after fabrication, making the process compatible with subsequent standard semiconductor processing. N-type, p-type, and shielded polysilicon filled versions were demonstrated and modeled. These ETWI are CMOS compatible, and particularly appropriate for integration with released silicon sensors, such as cantilever and membrane arrays.

Acknowledgment

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References

[1] S. F. AlSarawi, D. Abbott, and P. D. Franzon, "A review of 3-D packaging technology," *IEEE Trans. Compon. Packag. Manufact. Technol. Part B—Adv. Packag.*, vol. 21, pp. 2–14, 1998.

[2] M. Heschel, J. F. Kuhmann, S. Bouwstra, and M. Amskov, "Stacking technology for a space constrained microsystem," *J. Intell. Mater. Syst. Struct.*, vol. 9, pp. 749–754, 1998.

[3] J. H. Wu, J. A. del Alamo, and K. A. Jenkins, "A high aspect-ratio silicon substrate-via technology and applications: Through-wafer interconnects for power and ground and faraday cages for SOC isolation," in *Proc. International Electron Devices Meeting*, San Francisco, CA, 2000, pp. 477–480.

[4] H. Furukawa, T. Fukui, T. Tanaka, A. Noma, and D. Ueda, "A novel fabrication process of surface via-holes for GaAs power FETS," in *20th Annual Gallium Arsenide Integrated Circuit Symposium Technical Digest*, 1998, pp. 251–254.

[5] K. M. Strohm, P. Nuechter, C. N. Rheinfelder, and R. Guehl, "Via hole technology for microstrip transmission lines and passive elements on high resistivity silicon," in *IEEE MTT-S International Microwave Symposium*, Anaheim, CA, 1999, pp. 581–584.

[6] H. T. Soh, C. P. Yue, A. McCarthy, C. Ryu, T. H. Lee, S. S. Wong, and C. F. Quate, "Ultra-low resistance, through-wafer via (TWV) technology and its applications in three dimensional structures on silicon," *Jpn. J. Appl. Phys., Part 1 (Regular Papers, Short Notes & Review Papers)*, vol. 38, pp. 2393–2396, 1999.

[7] N. Takahashi, N. Senba, Y. Shimada, I. Morisaki, and K. Tokuno, "Three-dimensional memory module," *IEEE Trans. Compon. Packag. Manufact. Technol. Part B—Adv. Packag.*, vol. 21, pp. 15–19, 1998.

[8] S. Linder, "Chip stacks for memory applications," Ph.D. dissertation, Swiss Federal Institute of Technology in Physical Electronics Laboratory, 1996.

[9] S. Souri, K. Banerjee, A. Mehrotra, and K. Saraswat, "Multiple Si layer ICs: Motivation, performance analysis, and design implications," in *Proc. 2000, 37th Design Automation Conference,*, 2000, pp. 213–220.

[10] E. M. Chow, H. T. Soh, H. C. Lee, J. D. Adams, S. C. Minne, G. Yaralioglu, A. Atalar, C. F. Quate, and T. W. Kenny, "Two-dimensional cantilever arrays with through-wafer interconnects," in *Proc. 10th International Conference on Solid-State Sensors and Actuators*, Sendai, Japan, 1999, pp. 1886–1887.

[11] ——, "Integration of through-wafer interconnects with a two-dimensional cantilever array," *Sens. Actuators A, Phys.*, vol. 83, pp. 118–123, 2000.

[12] E. M. Chow, G. G. Yaralioglu, C. F. Quate, and T. W. Kenny, "Characterization of a two-dimensional cantilever array with through-wafer electrical interconnects," *Appl. Phys. Lett.*, vol. 80, pp. 664–666, 2002.

[13] H. D. Goldberg, K. S. Breuer, and M. A. Schmidt, "A silicon wafer-bonding technology for microfabricated shear-stress sensors with backside contacts," in Solid-State Sensor and Actuator Workshop, Hilton Head Island, SC, 1994.

[14] D. W. Lee, T. Ono, T. Abe, and M. Esashi, "Fabrication of microprobe array with sub-100nm nano-heater for nanometric thermal imaging and data storage," in *Proc. 14th IEEE International Conference on Micro Electro Mechanical Systems (MEMS2001)*, Interlaken, Switzerland, 2001, pp. 204–207.

[15] X. C. Jin, S. Calmes, C. H. Cheng, F. L. Degertekin, and B. T. Khuri-Yakub, "Micromachined capacitive ultrasonic immersion transducer array," in *Proc. 10th International Conference on Solid-State Sensors and Actuators (Transducers '99)*, Sendai, Japan, 1999, pp. 1500–1503.

[16] C. H. Mastrangelo, M. A. Burns, and D. T. Burke, "Microfabricated devices for genetic diagnostics," *Proc. IEEE*, vol. 86, pp. 1769–1787, 1998.

[17] D. R. Baselt, G. U. Lee, and R. J. Colton, "Biosensor based on force microscope technology," *J. Vacuum Sci. Technol. B*, vol. 14, pp. 789–793, 1996.

[18] V. Chandrasekaran, E. M. Chow, T. W. Kenny, T. Nishida, L. Cattafesta, B. Sankar, and M. C. Sheplak, "Thermoelastically actuated acoustic proximity sensor with integrated through-wafer interconnects," in Solid-State Sensor and Actuator Workshop, Hilton Head Island, SC, 2002.

[19] D. Hulsenberg, "Glasses for microsystems technology," *Microelectron. J.*, vol. 28, pp. 419–432, 1997.

[20] P. F. Indermuhle, E. Ammann, P. Haring, R. Kotz, H. Siegenthaler, and N. F. deRooij, "Electrolytic thin layer scanning tunneling microscope: Fabrication and first results," *Microelectron. Eng.*, vol. 42, pp. 547–550, 1998.

[21] H. Yamada, T. Togasaki, M. Kimura, and H. Sudo, "High-density 3D packaging technology for CCD micro-camera system module," in *Proc. 14th IEEE International Conference on Micro Electro Mechanical Systems*, Interlaken, Switzerland, 2001, pp. 14–17.

[22] X. Li, T. Abe, Y. Liu, and M. Esashi, "High density electrical feedthrough fabricated by deep reactive ion etching of pyrex glass," in *Proc. 14th IEEE International Conference on Micro Electro Mechanical Systems*, Interlaken, Switzerland, 2001, pp. 98–101.

[23] T. R. Anthony, "Forming electrical interconnections through semiconductor wafers," *J. Appl. Phys.*, vol. 42, pp. 5340–5349, 1981.

[24] C. Christensen, P. Kersten, S. Henke, and S. Bouwstra, "Wafer through-hole interconnections with high vertical wiring densities," *IEEE Trans. Compon., Packag., Manufact. Technol., Part A*, vol. 19, pp. 516–522, 1996.

[25] S. Linder, H. Baltes, F. Gnaedinger, and E. Doering, "Fabrication technology for wafer through-hole interconnections and three-dimensional stacks of chips and wafers," in *Proc. IEEE Micro Electro Mechanical Systems. An Investigation of Micro Structures, Sensors, Actuators, Machines and Robotic Systems*, New York, NY, 1994, (Cat. no. 94CH3404-1), pp. 349–354.

[26] G. J. Burger, E. J. T. Smulders, J. W. Berenschot, T. S. J. Lammerink, J. H. J. Fluitman, and S. Imai, "High-resolution shadow-mask patterning in deep holes and its application to an electrical wafer feed-through," *Sens. Actuators A, Phys.*, vol. 54, pp. 669–673, 1996.

[27] S. Savastiouk, "Moore's Law: The z dimension," *Solid State Technol.*, vol. 43, p. 84, 2000.

[28] N. P. Pham, K. T. Ng, M. Bartek, P. M. Sarro, B. Rejaei, and J. N. Burghartz, "A micromachining post-process module for RF silicon technology," in *Proc. International Electron Devices Meeting*, San Francisco, CA, 2000, pp. 481–484.

[29] E. M. Chow, H. T. Soh, A. Partridge, J. A. Harley, T. W. Kenny, C. F. Quate, S. Abdollahi-Alibeik, J. P. McVittie, and A. McCarthy, "Fabrication of high-density cantilever arrays and through-wafer interconnects," in *Solid-State Sens. Actuator Workshop*, Hilton Head Island, 1998, pp. 220–224.

[30] C. Kenney, S. Parker, J. Segal, and C. Storment, "Silicon detectors with 3-D electrode arrays: Fabrication and initial test results," *IEEE Trans. Nuclear Sci.*, vol. 46, pp. 1224–1236, 1999.

[31] E. M. Chow, A. Partridge, C. F. Quate, and T. W. Kenny, "Through-wafer electrical interconnects compatible with standard semiconductor processing," in *Solid-State Sens. Actuator Workshop*, Hilton Head Island, SC, 2000, pp. 343–346.

[32] V. Chandrasekaran, E. M. Chow, T. W. Kenny, T. Nishida, and M. Sheplak, "Through-wafer electrical interconnects for MEMS sensors," in *Proc. 2001 ASME International Mechanical Engineering Congress and Exposition*, New York, 2001.

[33] C. H. Cheng, E. M. Chow, X. Jin, S. Ergun, and B. T. Khuri-Yakub, "An efficient electrical addressing method using through-wafer vias for two-dimensional ultrasonic arrays," in *2000 IEEE International Ultrasonics Symposium*, San Juan, Puerto Rico, 2000, pp. 1179–1182.

[34] C. H. Cheng, A. S. Ergun, and B. T. Khuri-Yakub, "Electrical through-wafer interconnects with 0.05 pico farads parasitic capacitance on 400 μm thick silicon substrates," in *Solid-State Sensor and Actuator Workshop*, Hilton Head Island, SC, 2002, pp. 157–160.

[35] S. C. Minne, S. R. Manalis, and C. F. Quate, "Parallel atomic-force microscopy using cantilevers with integrated piezoresistive sensors and integrated piezoelectric actuators," *Appl. Phys. Lett.*, vol. 67, pp. 3918–3920, 1995.

[36] B. J. Kane, M. R. Cutkosky, and G. T. A. Kovacs, "A traction stress sensor array for use in high-resolution robotic tactile imaging," *J. Microelectromech. Syst.*, vol. 9, pp. 425–434, 2000.

[37] F. Laermer and A. Schilp, "Method of anisotropically etching silicon," U.S. Patent no. 5 501 893, 1996.

[38] A. A. Ayon, R. Braff, C. C. Lin, H. H. Sawin, and M. A. Schmidt, "Characterization of a time multiplexed inductively coupled plasma etcher," *J. Electrochem. Soc.*, vol. 146, pp. 339–349, 1999.

[39] J. Bhardwaj, H. Ashraf, A. McQuarrie, G. Barna, and H. G. Hughes, "Dry silicon etching for MEMS," in *Proc. Third International Symposium on Microstructures and Microfabricated Systems*, Pennington, NJ, 1997, pp. 118–130.

[40] R. A. Gottscho, C. W. Jurgensen, and D. J. Vitkavage, "Microscopic uniformity in plasma etching," *J. Vacuum Sci. Technol. B (Microelectron. Nanometer Struct.)*, vol. 10, pp. 2133–2147, 1992.

[41] T. Kamins, *Polycrystalline Silicon for Integrated Circuits and Displays*, 2nd ed. Boston, MA: Kluwer Academic, 1998.

[42] E. M. Chow, "Electrical through-wafer interconnects and microfabricated cantilever arrays using through-wafer silicon etching," Ph.D. dissertation, Stanford University, CA, 2001.

[43] M. J. Deen, S. Rumyantsev, and J. Orchard-Webb, "Low frequency noise in heavily doped polysilicon thin film resistors," *J. Vacuum Sci. Technol. B (Microelectron. Nanometer Struct.)*, vol. 16, pp. 1881–1884, 1998.

[44] V. Subramanian and K. C. Saraswat, "High-performance germanium-seeded laterally crystallized TFT's for vertical device integration," *IEEE Trans. Electron Devices*, vol. 45, pp. 1934–1939, 1998.

[45] X. Y. Chen and C. Salm, "Doping dependence of low-frequency noise in polycrystalline SiGe film resistors," *Appl. Phys. Lett.*, vol. 75, pp. 516–518, 1999.
[46] A. E. Franke, Y. Jiao, M. T. Wu, T. J. King, and R. T. Howe, "Post-CMOS modular integration of poly-SiGe microstructures using poly-Ge sacrificial layers," in *Solid-State Sens. Actuator Workshop*, Hilton Head Island, SC, 2000, pp. 18–21.

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Electrical Through-Wafer Interconnects with Sub-PicoFarad Parasitic Capacitance

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***Abstract*-This paper presents a technology for high density and low parasitic capacitance electrical through-wafer interconnects to an array of capacitive micromachined ultrasonic transducers (CMUTs) on a silicon wafer. Vertical wafer feedthroughs (interconnects) connect an array of sensors or actuators from the front side (transducer side) to the backside (packaging side) of the wafer. A 20 to 1 high aspect ratio 400 μm long and 20 μm diameter interconnect is achieved by using deep reactive ion etching (DRIE). Reduction of the parasitic capacitance of the polysilicon pads to the substrate can be achieved by using reversed-biased pn-junction diodes operating in the depletion region. A parasitic capacitance of 0.3 pF has been achieved by this means. This three-dimensional architecture allows for elegant packaging through simple flip-chip bonding of the chip's back side to a printed circuit board (PCB) or a signal processing wafer.**

I. Introduction

One of the main problems in fabricating two-dimensional ultrasonic transducer arrays is the addressing of the individual array elements [1][2][3]. If the array size is large, a significant sacrifice in the array element area is required if the addressing is done through a routing network. Although ultrasonic transducers are considered here, this problem is a challenge for any kind of array fabrication. This paper presents a solution with technology that provides electrical interconnects to arrays of micro-electro mechanical systems (MEMS) devices on a silicon wafer.

The architecture is based on through-wafer vertical interconnects with high aspect ratio. Many processes have been previously used to fabricate through-wafer interconnects [4][5] including dry etched polysilicon filled interconnects by Chow et al [6]. For our previous work, we have integrated similar interconnects into an active sensor array and made improvements on a parasitic capacitance of 2.67 pF [7].

In an ultrasonic transducer array operation, the parasitic capacitance of the interconnect between an array element and its electronics is the limiting factor for the dynamic range and frequency bandwidth. Therefore, it is always best to put the electronics as close to the array elements as possible. In this work, we demonstrate a way to integrate a 128 x 128 capacitive micromachined ultrasonic transducer (CMUT) array with the electronic circuits without sacrificing the performance of either one and minimizing the parasitic capacitance. To do this, an electrical through-wafer interconnect (ETWI) is employed to address the array elements individually (Fig. 1), where the front side of the wafer is fully populated with the ultrasonic array elements, and the backside is solely dedicated to bond pads for the flip-chip bonding to the printed circuit board (PCB) or the integrated circuits (Fig. 1). In this way, the parasitics due to any interconnection cable are avoided. To further improve the device performance, the parasitic capacitance of the ETWI to the silicon substrate needs to be reduced to a comparatively lower level than the device capacitance.

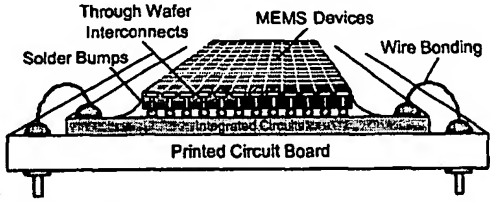

Fig. 1. Packaging schematics of through-wafer interconnects.

II. Parasitic Capacitance Reduction

Parasitic capacitance has a detrimental effect on the performance of the CMUT. For each array element, there are three sources contributing to the parasitic capacitance, the front side 400 μm x 400 μm pad for the bottom electrode of the transducers, the backside 200 μm x 140 μm pad for bonding, and the through-wafer interconnect with 400 μm length and 20 μm diameter (Fig. 2). The optimum solution for the parasitic capacitance reduction is to implement reverse-biased pn-junction diodes on the front and backside pads of the wafer and reverse-biased metal-insulator-semiconductor (MIS) junction inside the interconnects as shown in Fig. 3. Since the silicon substrate is ground, the pads and the through-wafer interconnects have a capacitance with related to the substrate. When the pn junction is applied with a reversed DC bias, the high resistivity (> 1000 ohm-cm) silicon substrate is fully depleted from electrons, thus a low parasitic capacitance is achieved.

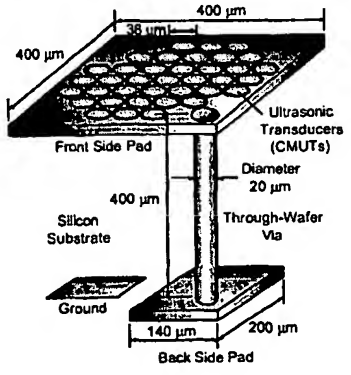

Fig. 2. pn- junction through wafer interconnect schematics.

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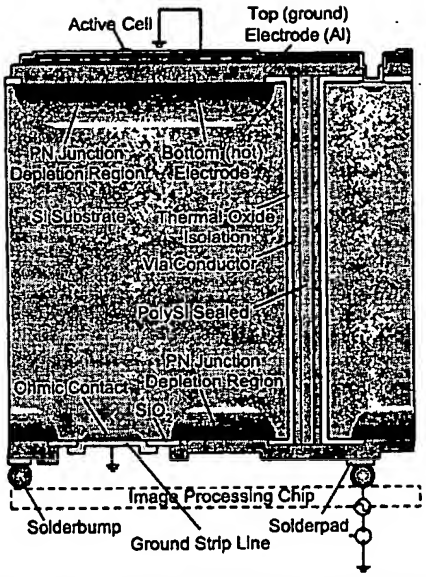

Fig. 3. pn-junction through wafer Interconnect cross section.

III. Expected Parasitic Capacitance

Based on the simulation (Fig. 4), a silicon substrate with resistivity of 1000 ohm-cm is used. A reversed bias voltage of 50 volts is applied to drive the pn-junction diodes into the depletion region. The calculated pn-junction depletion region length is 119 μm. Although the MIS through-wafer interconnect depletion region length is only 9.26 μm, the depletion region of the pn-junction pads can also spread into the substrate near the through-wafer interconnect that the parasitic capacitance of the through-wafer interconnect is further reduced on the regions near both pads. We expect a total parasitic capacitance of 0.234 pF including the front and back side pads and a single through-wafer interconnect which is a substantial improvement compared to the previous result reported [7].

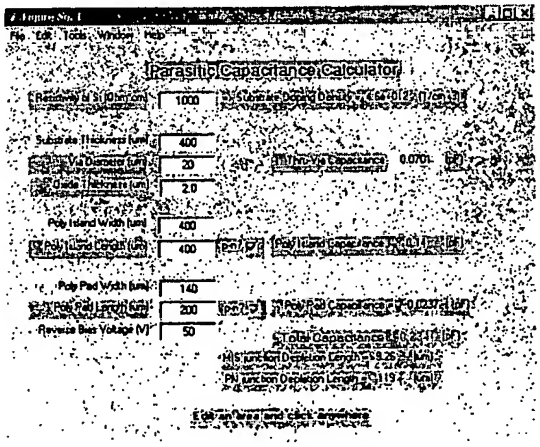

Fig. 4. Expected parasitic capacitance.

IV. Through Wafer Intrconnect Process

The process flow is shown in Fig. 5. We start with a 400 μm thick double-sided polished n-type <100> Si wafer which is thermally oxidized to 2 μm thick to serve as a hard mask for the deep etch. Both sides are then patterned with 20 μm diameter openings for each interconnect. The through-wafer deep etch is done by etching half way from both sides of the wafer (Fig. 5a). By this means, a 20 to 1 high aspect ration via hole can be achieved. When the interconnect is etched through, the helium flow used for cooling goes through the etched holes, and the etching will be slowed down, serving as an etch stop. The oxide mask is then removed by buffered oxide etch (BOE). For MIS isolation at locations with no pn junction, the wafer is thermally oxidized to 1 μm (Fig. 5b). A layer of 2 μm polysilicon is deposited and then heavily doped with boron to enhance the conductance (Fig..5c). A layer of low temperature oxide (LTO) is deposited to serve as an etching stop for the etch-back of polysilicon deposited in the following step. The interconnect holes are then filled with polysilicon (Fig. 5d). The polysilicon on both sides is then etched back and stopped on the LTO (Fig. 5e). After removing the LTO, the 2 μm doped polysilicon is exposed again and ready to be etched for the front and back side oxide opening (Fig. 5f). Another layer of 0.5 μm polysilicon is deposited and doped with boron which makes up the pn junctions (Fig. 5g). The front and back side polysilicon pads are patterned followed by the oxide etch on the back side for ground opening and heavily doped for ohmic contact. After this step, the ultrasonic transducers (CMUTs) can be built on top of the front side polysilicon (Figs. 6 and 7). At the very end, the back side metal pads for flip-chip bonding are formed by lift-off (Fig. 8). The SEM pictures show the cross section of a finished interconnect in Fig. 9. The wafer is ready for flip-chip bonding to a circuit chip or PCB.

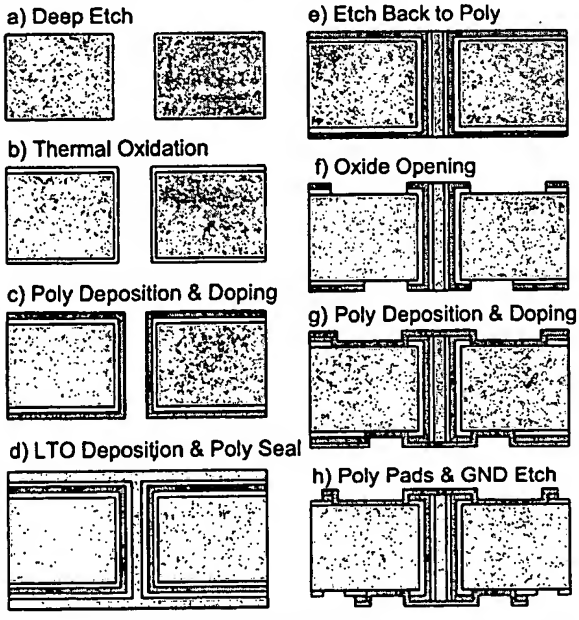

Fig. 5. Fabrication process for through-wafer interconnects.

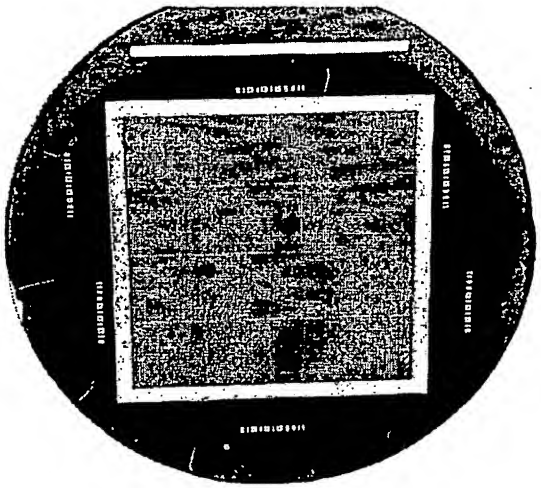

Fig. 6. Photograph of a finished 128 x 128 CMUT array on a 4" silicon wafer.

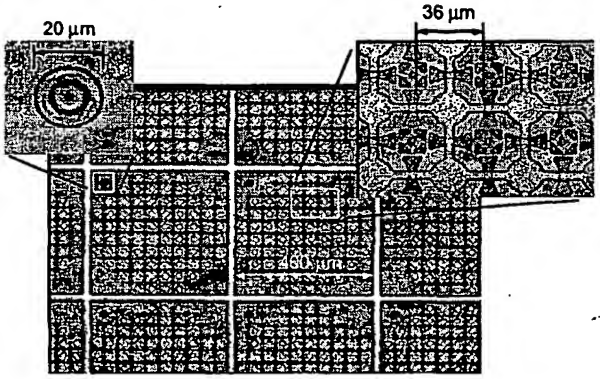

Fig. 7. Photograph of the CMUT array elements with interconnects.

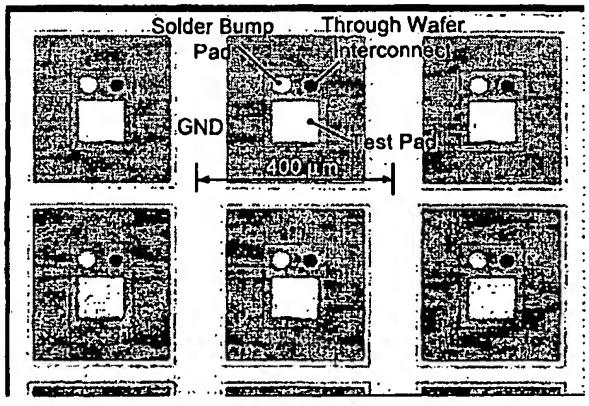

Fig. 8. Photograph of the wafer backside.

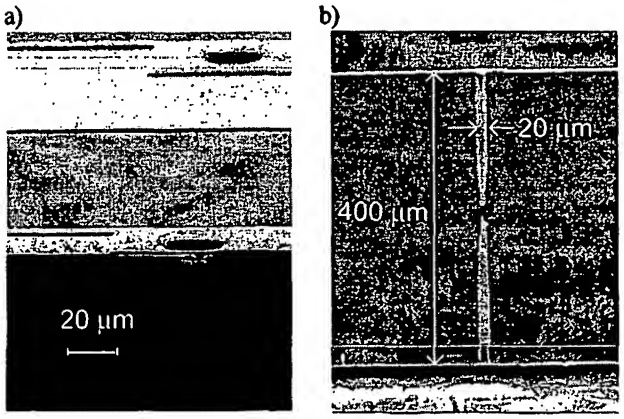

Fig. 9. SEM picture of the cross section of the interconnects.

V. Test Results

A. C-V Characterization of Through-Wafer Interconnects with PN-Junction Pads

As shown in Fig. 10, a testing device with a through-wafer interconnect connected with both front side and back side pads and a ground to the substrate is employed to measure the C-V characteristic at 1 MHz frequency. A reversed DC bias is applied to drive both pn-junction pads into the depletion region. The total capacitance is the capacitance of the through-wafer interconnect plus both pads.

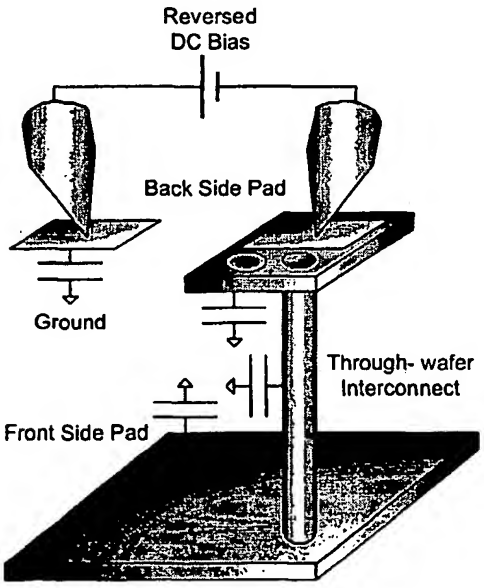

Fig. 10. Capacitance measurement set-up.

Fig. 11 shows a C-V characteristics at 1 MHz frequency. By applying a reverse bias for more than 5 volts the capacitance will decrease to 0.3 pF because of depletion into the substrate. This experimental result is very close to what we expected from the simulation.

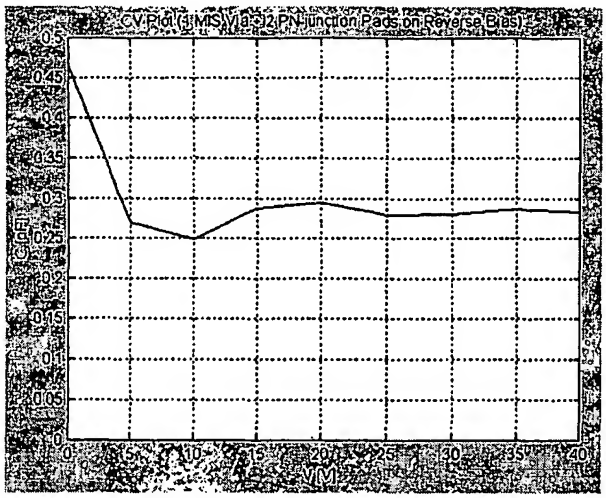

Fig. 11. Measured C-V curve of through-wafer interconnects

B. Impedance Measurement of CMUTs with Interconnects

The experimental setup is similar to that of the CV measurement but with integrated CMUTs on the front side pad. Fig. 12 shows the input impedance of a CMUT array element connected to the wafer back side with an interconnect operating at 20 volts applied bias. The acoustical resonance behavior of the CMUT shows that the through-wafer interconnects are indeed working. However, note that there is a baseline of around 130 ohm in the impedance characteristic which is due to the series resistance of the through-wafer interconnects.

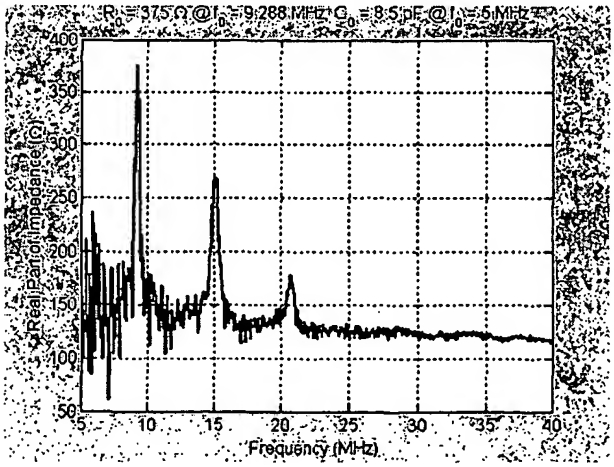

Fig. 12. Impedance measurement of CMUTs with through -wafer interconnects.

VI. Conclusion

Both C-V and impedance measurements reveal that electrical through-wafer interconnects with very low parasitic capacitance have been achieved. Although the series resistance of the through-wafer interconnects is not very serious for the CMUT application, it stands as a problem for the future. This series resistance can be substantially reduced by employing multiple polysilicon deposition and boron doping cycles at step c of Fig. 5 which will be shown in a future work.

Acknowledgment

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References

[1] B. T. Khuri-Yakub, C. H. Cheng, F. L. Degertekin, S. Ergun, S. Hansen, X. C. Jin, and O. Oralkan, "Silicon Micromachined Ultrasonic Transducers," presented at the Fifth European Conference on Underwater Acoustics, Lyon France, July 10-13, 2000.

[2] S. Calmes, C. H. Cheng, F. L. Degertekin, X. C. Jin, and B. T. Khuri-Yakub, "Highly Integrated 2-D Capacitive Micromachined Ultrasound Transducers," presented at the 1999 IEEE International Ultrasonics Symposium, Lake Tahoe, Nevada, Octobor 17-20, 1999; in Ultrasonics Symposium Proceedings, pp. 1163-6.

[3] X. C. Jin, C. H. Cheng. O. Oralkan, S. Calmes, F. L. Degertekin, and B. T. Khuri-Yakub, "Recent Progress in Capacitive Micromachined Ultrasonic Immersion Transducer Array," presented at the 8th International Symposium on Integrated Circuits, Devices and Systems, Singapore, September 8-10, 1999; in ISIC-99 Proceedings, pp.159-162.

[4] H. T. Soh, C. P. Yue, A. McCarthy, et al., "Ultra-Low Resistance, Through-Wafer Via (TWV) Technology and Its Application in Three Dimensional Structures on Silicon," Japanese Journal of Applied Physics, Part I 38(4B), 2393-6 (1999).

[5] T. R. Anthony, "Forming Electrical Interconnections through Semiconductor Wafers," Journal of Applied Physics, 52(8) 5340-9 (1981).

[6] E. M. Chow, A. Partridge, C. F. Quate, T. W. Kenny, "Through-Wafer Electrical Interconnects Compatible with Stanford Semiconductor Processing," Solid-State Sensor and Actuator Workshop, Hilton Head Island, South Carolina, June 4-8, 2000, pp. 343-6.

[7] C. H. Cheng, E. M. Chow, A. S. Ergun, B. T. Khuri-Yakub, "An Efficient Electrical Addressing Method Using Through-Wafer Vias for Two-Dimensional Ultrasonic Arrays," 2000 IEEE International Ultrasonics Symposium, San Juan, Puerto Rico, October 22-25, 2000; in Ultrasonics Symposium Proceedings, pp. 1179-1182.

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THROUGH-WAFER ELECTRICAL INTERCONNECTS FOR MEMS SENSORS

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ABSTRACT

The fabrication and characterization of p-type silicon electrical through-wafer interconnects (pETWI) on a silicon wafer is presented. Together with previously developed n-type ETWI [1], the pETWI enables complementary ETWI (CETWI) for maximum flexibility of through-wafer interconnects for MEMS sensors and semiconductor devices. Deep reactive ion etching using the Bosch process is employed to create high aspect ratio 20 μm vias through the wafer. The interconnects are electrically isolated from the bulk silicon substrate by a 2 μm thermal oxide layer. Electrical conduction is achieved by depositing several layers of boron-doped polysilicon. Details of the fabrication process as well as results of the pETWI characterization are presented. Interconnects with various polysilicon doping concentrations were fabricated to investigate the effect on the resistance, capacitance and noise. Average resistance values between 10 Ω and 14 Ω were obtained for each interconnect depending on the doping levels. This resistance is suitable for many MEMS applications. High frequency capacitance versus voltage (C-V) characteristics and the noise power spectral density (PSD) were also measured.

INTRODUCTION

Recent advances in packaging technologies have shown the use of backside contacts as a viable alternative to conventional top-side wire bonding. In order to utilize backside contacts, electrical through-wafer interconnects are needed. Such contacts offer the advantage of replacing the top-side, wire-bonded electrical leads with "flip-chip" type solder-bump backside connections. By eliminating wire bonds on the front surface, a flush-mounted sensor may be fabricated with the electrical leads hidden from the environment. The backside contacts will also permit the simple bump-bond hybrid packaging of the sensor die onto a high-performance application-specific, integrated circuit (ASIC). The advantage of a backside packaging scheme include an increase in device reliability due to a reduction in the number of wire bonds, an increase in the density of interconnects, and a lower cost of assembly [2]. The bump-bond technique provides a much higher interconnection density than wire bonding because interconnects are distributed across the surface of the chip, instead of being restricted to the periphery.

Several different technologies have been employed for creating electrical through-wafer interconnects (ETWI). However, most of these techniques are incompatible with standard CMOS processing. Anisotropic wet chemical etching is a commonly used technique for micromachining the through-wafer vias, but this technique results in large chip sizes and impedes the subsequent processing with many etching, metallization and lithography equipment [3,4,5]. Copper electroplating methods have also been combined with deep reactive ion etching (DRIE) to form ETWI for RF applications [6,7,8]. DRIE has also been combined with chemical vapor deposition (CVD) tungsten for cantilever array applications [9]. Metal-filled DRIE-etched vias permit a smaller chip size, relative to the wet-etched contacts, but the metals used in the interconnects are not always compatible with high temperature processing, thus limiting the commercial use of these technique.

The technology to create high density, n-type polysilicon filled electrical through-wafer interconnects (nETWI) using

DRIE was demonstrated by *Chow et. al* [1]. Using this technique, 20 μm diameter vias with an aspect ratio of ~25:1 were achieved. Phosphorus-doped polysilicon forms the conducting layer, which is isolated from the substrate with a *2* μm thermal oxide. This technique is completely CMOS compatible and possesses several distinct advantages: the capability to withstand subsequent high temperature thin film deposition and device fabrication steps after ETWI fabrication and low resistance/capacitance suitable for MEMS applications.

This paper presents an extension to the nETWI by exploring the feasibility of p-type electrical through-wafer interconnects (pETWI). The ability to create both n and p-type interconnects enables complementary ETWI and would ultimately improve the flexibility of this polysilicon-level interconnection technology. For example, in the case of microfabricated mechanical sensors (e.g., diaphragms or cantilever beams), p-type piezoresistive strain gauges are commonly used. P-type ETWI enables direct ohmic contact to p-type piezoresistors, avoiding non-linear rectification created at the P/N junctions.

P-TYPE THROUGH WAFER INTERCONNECT DESIGN

The pETWI consists of a 20 μm-diameter via through a silicon substrate with an aspect ratio of ~ 20:1. The conductor is electrically isolated from the bulk substrate by a 2 μm thermal oxide. Multiple conformal layers of boron-doped polysilicon are deposited to form the actual electrical conductor. The overall resistance of the interconnect is determined by the geometry and the level of polysilicon doping. **Figure 1** shows the top-view of the polysilicon pETWI integrated with an aluminum pad.

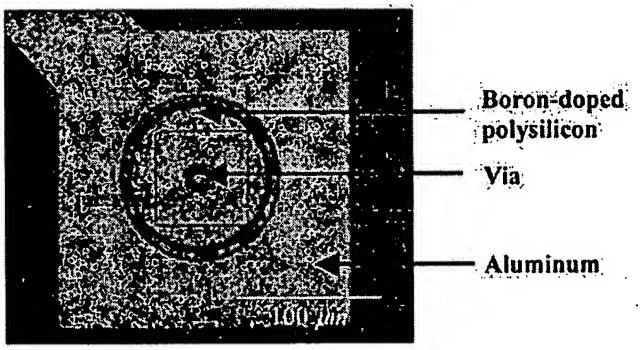

Figure 1: Optical micrograph of polysilicon pETWI integrated with a metal pad.

The pETWI fabrication process begins with a 450 μm thick double polished n-type silicon-on-insulator wafer as illustrated in **Figure 2.**

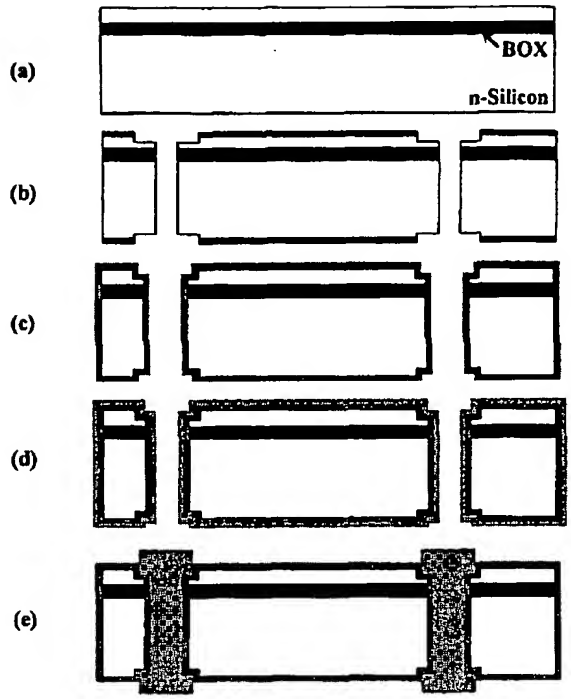

Figure 2: Schematic of the electrical through-wafer interconnect fabrication process a) Starting silicon-on-insulator wafer. b) Holes etched through the wafer. c) Insulating thermal oxide grown. d) Polysilicon is deposited, diffusion doped and annealed. e) Additional polysilicon is deposited to fill and the conducting polysilicon layer is patterned on both sides.

A 2 μm thermally grown silicon dioxide acts as the mask for the through-wafer via etch. In order to maintain a high aspect ratio structure, the vias are created by etching through both sides of the wafer. A front-side etch is used halfway through the wafer followed by an etch from the backside to complete the via. The front to back alignment of the via pattern is critical to achieve a straight profile. A front to back aligner is used to create the aligned two-sided pattern on the wafer. Additionally, an IR camera is used to inspect the alignment before the etch. A slight misalignment would result in a reduction of the via diameter, causing it to prematurely plug during the deposition of the polysilicon thin films. A deep reactive ion etch (Surface Technology Systems) is performed from the front and the backside of the wafer for roughly equal durations to etch the via. The etcher uses the Bosch process alternating between etching and passivation to create a high aspect ratio structure. Once the via is etched through the backside, helium used for cooling flows through the via slowing the etch. By monitoring the helium flow, we can estimate the etch progress. A small degree of lateral etching results in a V-shaped (gradually reducing diameter) via profile towards the center of the wafer, as illustrated in **Figure 3.** A 30 *min* timed

overetch is performed from the front side of the wafer using an etch recipe with higher passivation to smooth and straighten out the via profile. A support wafer is used for the overetch to prevent helium flow into the vias. Once the vias are etched, the oxide mask is stripped using a buffered oxide etch (BOE).

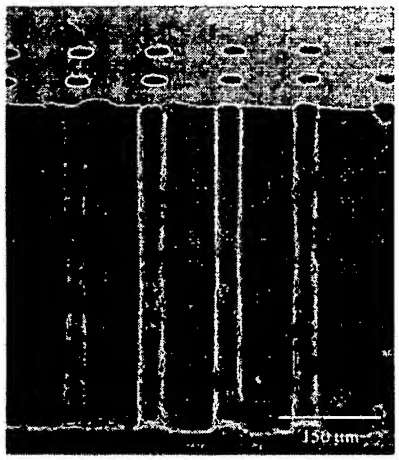

Figure 3: SEM cross-section after plasma etching vias through the wafer [1].

The via etch step is followed by conformal thin film deposition. To electrically isolate the interconnect from the bulk silicon substrate, a 2 μm thermal oxide is grown using a dry-wet-dry oxidation process. The dry-wet-dry oxidation process is used to ensure a quality silicon-to-silicon dioxide interface.

For electrical conduction, 2 μm LPCVD polysilicon is deposited over the oxide. This is followed by boron diffusion doping of the polysilicon for 2 hours at 1000°C and then an anneal at 1000°C to fully drive the dopants through the polysilicon. The boron diffusion doping of polysilicon forms a non-conducting borosilicate glass, which is not easily removed using hydrofluoric acid. This is a critical difference between boron (p-type) and phosphorus (n-type) diffusion doping. The glass resulting from phosphorus doping of polysilicon is easily etched using hydrofluoric acid. However, in the case of polysilicon doping using boron, the glass must first be oxidized using wet oxidation at 1100°C for 30 minutes, then followed by 60 minutes in (6:1) BOE to etch the oxidized glass. It is not clear whether the BOE etch completely removes the borosilicate inside the vias, in which case a thin layer of non-conducting oxide may be present in the vias. If the oxide is completely etched on the surface and at the opening of the vias on both sides, then we can model the ETWI as a stack of concentric resistors, which can perform just as efficiently. The process of polysilicon deposition and boron diffusion doping is repeated 2-3 times to achieve a low resistance pETWI.

EXPERIMENTAL SETUP

The experiments were carried out in the Interdisciplinary Microsystems Laboratory at the University of Florida. Measurements were made on different pETWI interconnect chains connected in series by surface (400 μm long and 100 μm wide) p-type polysilicon lines. Measurements included current vs. voltage (I-V) to investigate the ohmic behavior of the ETWI, capacitance vs. voltage (C-V) to test the isolation characteristics of the silicon dioxide, and noise PSD to determine the effect of the interconnect on the sensor performance. Measurements were made on multiple devices, to obtain statistical measures of each of the parameters.

Current vs. Voltage

Current versus voltage (I-V) characterizations were performed on different pETWI chains to determine the device resistance. The measurements were made using a Hewlett Packard 4155B semiconductor parameter analyzer and a wafer level probe station. Bias voltage ranging from –10 V to 10 V (0.1 V increments) was applied across the ETWI chain, while monitoring the current at each step. This process was repeated for different lengths pETWI chains (specifically 6, 22 and 62 ETWI in series) to arrive at an average resistance value for a single pETWI.

Capacitance vs. Voltage

Interconnect capacitance affects the propagation delay of signals as well as the capacitive loading of the sensor output. The p-type polysilicon interconnect dielectrically isolated from the n-type substrate forms a metal-oxide-semiconductor capacitor (MOSC) where the polysilicon acts as a metal gate and the top silicon layer is the substrate. The voltage-dependent MOSC capacitance is characterized using a Hewlett Packard 4294A vector impedance meter at 1 MHz small signal frequency. Similar to the I-V characterization, the bias voltage (in this case, across the pETWI and the substrate) was swept from –20 V to 20 V (0.1 increments), while monitoring the capacitance at each voltage step. An open and short circuit calibration, prior to the measurements, was performed with the vector impedance meter to eliminate the capacitive contribution of the connecting leads and the test setup.

Noise Power Spectral Density

Since one application of an ETWI is the connection of sensor small-signal output to nearby signal-conditioning electronics, the noise contributed by the interconnect must be minimal. The noise floor of the pETWI was characterized using a Faraday cage and low-noise test equipment.

The aim of the experimental setup is to isolate the random physical noise of the device under test (DUT) from the deterministic interference. This is achieved via careful shielding and grounding. Deterministic sources arise from capacitive coupling of electromagnetic interference (EMI) to the device and cabling, with the AC wall power being the major contributor (60 Hz and its harmonics). The Faraday cage considerably reduces the interference, permitting analysis of the noise PSD via post processing.

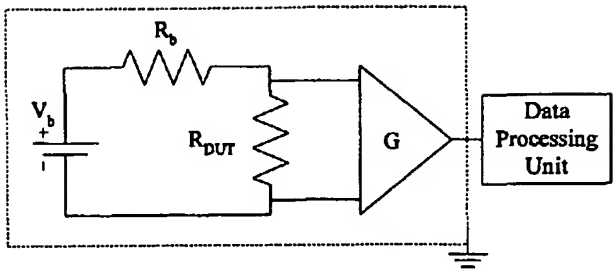

Figure 4: Schematic representation of the pETWI noise measurement setup. R_{DUT} represents the ETWI and R_b is the biasing resistor.

As illustrated in Figure 4, a battery powered Stanford Research Systems SR560 differential amplifier with specified noise voltage of 4 $nV/\sqrt{Hz}$ is used to amplify the differential voltage from the DUT using a gain of 10,000. This in conjunction with a battery (9 *V*) as the voltage source effectively eliminates the 60 *Hz* line interference. The voltage noise power spectral density was measured using a Stanford Research Systems SR785 spectrum analyzer after 500 averages. A frequency range of 0-10 *kHz* with a 2 *Hz* bin was used for recording the data. The voltage noise PSD of the interconnect is later extracted from the overall measured noise PSD of the circuit.

RESULTS AND DISCUSSION

The results of I-V, C-V and noise PSD characterizations are presented in this section.

Current vs. Voltage Characteristics

The interconnects display ohmic behavior as indicated by the linear variation of current and voltage in Figure 5. Average resistance values ranging from 10 Ω to 14 Ω were obtained for each interconnect depending on the doping levels as shown in Figure 6. This is comparable to the n-type ETWI (*14* Ω [9]) and is low enough for many MEMS applications. Low and high-doped pETWI were achieved by varying the thickness of the conducting (boron-doped) polysilicon layers. Specifically, the low-doped pETWI consists of a 4 μm-thick doped polysilicon layer, whereas the thickness of the conduction layer is 6 μm in the case of the high-doped pETWI.

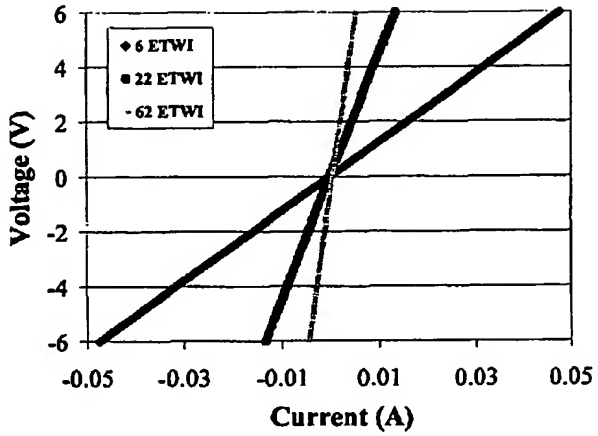

Figure 5: Current vs. voltage for chains of 6, 22 and 62 pETWI.

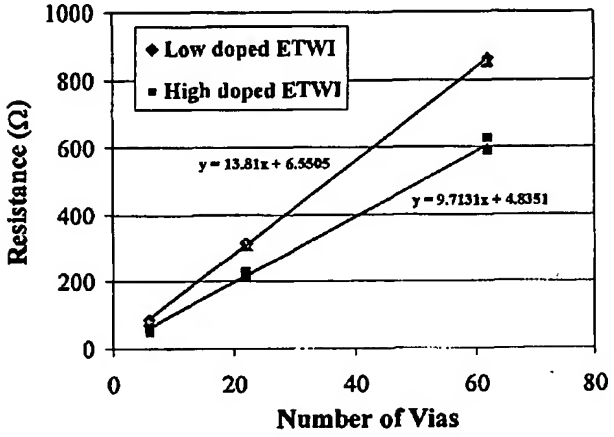

Figure 6: Plot showing the linear variation in resistance of the interconnects.

The theoretical minimum resistivity of p-type boron-doped polysilicon is 2000 $\mu\Omega$-*cm* [10], which corresponds to 25 Ω for a 20 μm diameter, 400 μm long conductor assuming uniform doping. However, an increase of 3 μm in the diameter can reduce the resistance to 12 Ω, that is consistent with our results. Although, the vias were designed to be 20 μm in diameter, several factors including mask erosion, overetch steps, simultaneous lateral etching can cause an increase in the diameter. In addition, doping crowding effects caused by oxidation can result in increased conduction.

Capacitance vs. Voltage Characteristics

The high frequency capacitance vs. voltage curve for varying bias voltage (-20 *V* to 20 *V*) between the substrate and the pETWI is shown in Figure 7. This high frequency capacitance-voltage curve is typical for a n-type substrate MOSC. An asymptotic maximum capacitance is observed at

large positive voltages when the n-type substrate is in accumulation and a minimum capacitance is seen at negative voltages when the substrate is inverted. The measured capacitance is lower than the theoretical ETWI capacitance due to the floating SOI substrate used in the pETWI process.

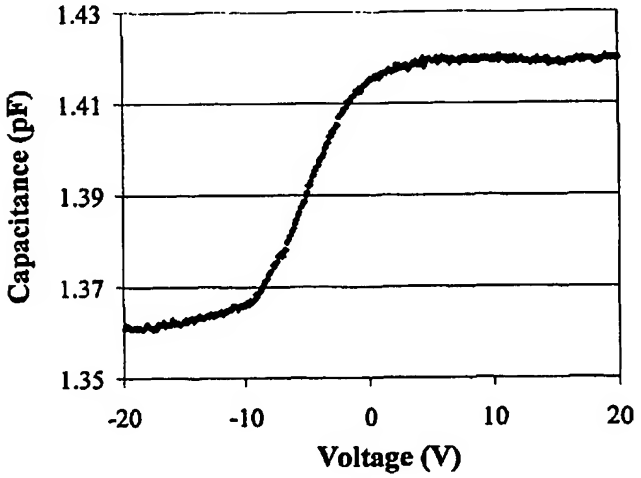

Figure 7: High-frequency capacitance vs. voltage characteristic of a 22 pETWI chain using a 1 MHz signal.

Noise Power Spectral Density

The voltage noise PSD of the pETWI is plotted in Figure 8. As indicated, the voltage noise PSD is dominated by *1/f* noise at low frequencies. The high *1/f* may be attributed in part to the heavily boron-doped polysilicon and also to the SOI structure where the bottom substrate was dielectrically isolated.

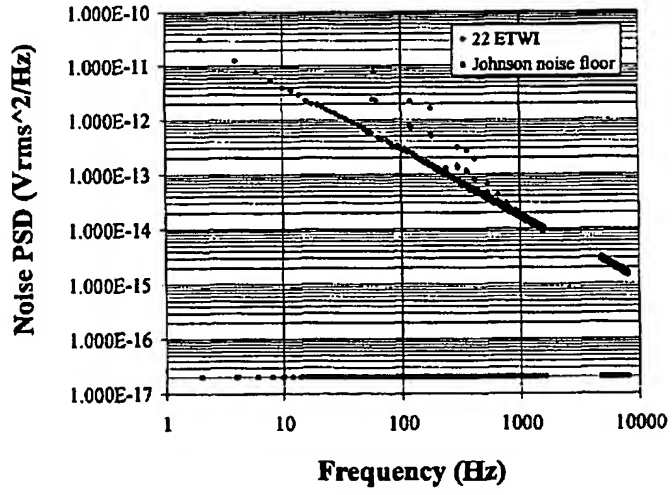

Figure 8: Noise PSD of the pETWI chain (with a total resistance of 1200 Ω).

CONCLUSIONS

A p-type electrical through-wafer interconnect has been developed and characterized, indicating low resistance and capacitance. These results indicate the feasibility of p-type electrical through-wafer interconnect (pETWI) to complement the nETWI previously developed. Together, the pETWI and nETWI enable a complementary ETWI technology, which provides flexibility for polysilicon-level backside interconnections for improved packaging reliability and high-density interconnects.

FUTURE WORK

The work presented here is a preliminary investigation into p-type ETWI for MEMS sensor/actuators. Accurate C-V characteristics and the device noise could not be extracted due to the lack of a proper contact to the bulk silicon substrate in the SOI wafer process. Future work will focus on fabrication process modifications to better suit a SOI wafer.

In-situ doped polysilicon deposition techniques will be explored for both the n-type (using a silane:phosphine:nitrogen mixture) and p-type (using a mixture of silane and boron-trichloride) ETWI and compared to the existing method in terms of via characteristics as well as deposition rates. Planarity is a critical issue for integration of the pre-process ETWI with an accompanying MEMS sensor/actuator. Techniques such as chemical mechanical polishing will be investigated towards this end.

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REFERENCES

1. Chow, E. M., Partridge, A., Quate, C. F., and Kenny, T. W., 2000, "Through-wafer electrical interconnects compatible with standard semiconductor processing", Solid State Sensors and Actuator Workshop, South Carolina, June 4-8, pp.343-6.

2. Heschel, M., Kuhmann, J. F., Bouwstra, S. and Amskov, M., 1998, "Stacking technology for a space constrained microsystem", Journal of Intelligent Material Systems and Structures, v. 9(9), pp. 749-54.

3. Goldberg, H.D., Breuer K.S., and Schmidt, M.A., 1994, "A silicon wafer-bonding technology for microfabricated shear-stress sensors with backside contacts," Technical Digest, Solid-State Sensor and Actuator Workshop, pp. 111-5.

4. Linder, S., Baltes, H., Gnaedinger, F., and Doering, E., 1994, "Fabrication technology for wafer through-hole

interconnections and three-dimensional stacks of chips and wafers", Proceedings IEEE Micro Electro Mechanical Systems. An Investigation of Micro Structures, Sensors, Actuators, Machines and Robotic Systems (Cat. No.94CH3404-1), New York, NY, USA, pp. 349-54.

5. Christensen, C., Kersten, P., Henke, S. and Bouwstra, S., 1996, "Wafer through-hole interconnections with high vertical wiring densities", IEEE Transactions on Components, Packaging, and Manufacturing Technology, Part A, v. 19(4), pp. 516-22.

6. Chow, E. M., Soh, H. T., Partridge, A., Harley, J. A., Kenny, T. W., and Quate, C. F., 1998, "Fabrication of high-density cantilever arrays and through-wafer interconnects", Solid-State Sensor and Actuator Workshop, South Carolina, June 8-11, pp. 220-4.

7. Soh, H. T., Yue, C. P., McCarthy, A., Ryu, C., Lee, T. H., Wong, S. and Quate, C. F., 1999, "Ultra-low resistance, through-wafer via (TWV) technology and its applications in three dimensional structures on silicon", Japanese Journal of Applied Physics, Part 1 (Regular Papers, Short Notes & Review Papers), v. 38(4B), pp. 2393-6.

8. Wu, J. H., del Alamo, J. A and Jenkins, K. A., 2000, "A high aspect-ratio silicon substrate via technology and applications: through-wafer interconnects for power and ground and faraday cages for SOC isolation," presented at International Electron Devices Meeting, San Fransisco, CA, pp. 477-480.

9. Chow, E. M., Soh, H. T., Lee, H. C., Adams, J. D., Minne, S. C., Yaralioglu, G., Atalar, A., Quate, C.F., Kenny, T. W., 2000, "Integration of through-wafer interconnects with a two-dimensional cantilever array", Sensors and Actuators, Physical A, v. 83(#1-3), MAY 22, pp. 118-23.

10. Kamins, T., 1998, *Polycrystalline silicon for integrated circuits and Displays*, 2nd Ed., Kluwer Academic Publishers, Boston, MA.

ELECTRICAL THROUGH-WAFER INTERCONNECTS AND MICROFABRICATED CANTILEVER ARRAYS USING THROUGH-WAFER SILICON ETCHING

A DISSERTATION
SUBMITTED TO THE DEPARTMENT OF ELECTRICAL ENGINEERING
AND THE COMMITTEE ON GRADUATE STUDIES
OF STANFORD UNIVERSITY
IN PARTIAL FULFILLMENT OF THE REQUIREMENTS
FOR THE DEGREE OF
DOCTOR OF PHILOSOPHY

Eugene Michael Chow

August 2001

I certify that I have read this dissertation and that in my opinion it is fully adequate, in scope and quality, as a dissertation for the degree of Doctor of Philosophy.

Thomas W. Kenny (Principal Advisor)

I certify that I have read this dissertation and that in my opinion it is fully adequate, in scope and quality, as a dissertation for the degree of Doctor of Philosophy.

Calvin F. Quate (Co-advisor)

I certify that I have read this dissertation and that in my opinion it is fully adequate, in scope and quality, as a dissertation for the degree of Doctor of Philosophy.

Butrus T. Khuri-Yakub

Approved for the University Committee on Graduate Studies:

Abstract

This work focuses on technology for electrical through-wafer interconnects (ETWI), cantilever arrays, and the integration of these two devices. Micromachined cantilevers are very sensitive and versatile sensors, with important applications in surface science, lithography, data storage, and biochemistry. To apply the capabilities of cantilevers over larger areas and with higher throughput, it is important to develop arrays. ETWI aid the fabrication of arrays of released sensors, such as cantilevers, because they address geometrical issues in alignment, electrical wiring, and density. ETWI also have broad applications for integrated circuits and micromachined sensors and actuators, as they permit three-dimensional design flexibility and facilitate system integration through wafer stacking.

Recent industry improvements of deep silicon etching techniques, based on a time multiplexed inductively coupled plasma (TMICP) etch process, now allow significantly increased aspect ratios (greater than 20:1) and depths (hundreds of microns). In this work, this etch technology is experimentally characterized and applied to silicon through-wafer applications. The problem of accurately releasing silicon sensors is addressed by combining TMICP etch processes with traditional plasma etching techniques.

The sensor release technique is then combined with an (ETWI) process to fabricate a novel two-dimensional array of sensors with backside electrical connections. The array consists of individually addressable piezoresistive cantilevers with high-aspect ratio tips. TMICP plasma etching is used to fabricate 30 μm diameter ETWI using tungsten and passive isolation, producing an unfilled via interconnect with ~1 Ω resistance. Mechanical and electrical characterization of the sensors is presented, as well as array operation as a microscope. This combination of cantilevers and interconnects enables operation of a high-density two-dimensional scanning probe array on large sample surfaces.

To simplify integration, improved ETWI are developed using a filled via of doped polysilicon. This interconnect is a passively isolated electrical through-wafer polysilicon plug, with a 20 μm diameter, 10-14 Ω resistance, and less than 1 pF capacitance. TMICP

plasma etching from both sides of the wafer is used to achieve an extremely high-aspect ratio etch (20:1 through 400 μm). The process is compatible with standard lithography, standard wafer handling, and high-temperature processing. N-type and p-type versions are demonstrated, and isolated ground planes are added to provide shielding against substrate noise. Electrical properties of these ETWI are measured and analytically modeled. These ETWI are currently being integrated with two types of ultrasound transducer arrays.

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List of Abbreviations

APC	Automatic Pressure Control
AR	Aspect Ratio
ARDE	Aspect Ratio Dependent Etching
BHF	Buffered Hydrofluoric Acid
BOE	Buffered Oxide Etch
CMUT	Capacitive Micromachined Ultrasound Transducers
CV	Capacitance-Voltage
CVD	Chemical Vapor Deposition
DRAM	Dynamic Random Access Memory
EDP	Ethylenediaminepyrocatechol
ETWI	Electrical Through-Wafer Interconnects
HDLP	High-Density Low-Pressure
HFCV	High-Frequency Capacitance-Voltage
HMDS	Hexamethyldisilazane
IC	Integrated Circuit
IV	Current Voltage
LFCV	Low-Frequency Capacitance-Voltage
LPCVD	Low-Pressure Chemical Vapor Deposition
MCM	Multi-Chip Module
MEMS	Micro-electro-mechanical systems
MOS	Metal Oxide Semiconductor
PGA	Pin Grid Array
SEM	Scanning Electron Microscope
SOI	Silicon On Insulator
STS	Surface Technology Systems, Inc.
TMAH	Tetramethylammoniumhydroxide
TMICP	Time Multiplexed Inductively Coupled Plasma
ZIF	Zero Insertion Force

Chapter 1: Introduction and Background

A dominant trend in microfabricated devices, both integrated circuits (IC) and micro-electro-mechanical systems (MEMS), is increased integration. By combining new materials and processes, researchers are steadily combining more and more capabilities onto a single chip. For example, microprocessors now come with on-chip memory, silicon radio frequency (RF) circuits are integrating the many blocks of a transceiver onto a single piece of silicon, and analog and digital circuits can be fabricated on the same chip.

If these electronics are combined with sensors, a smart transducer is possible. Arrays of microfabricated arrays could sense trace chemical quantities, analyze the signals, store them, and then communicate them to remote stations [1, 2]. Imaging arrays combined with the support electronics would enable micro-digital cameras with broad applications in medicine, automobiles, security, toys, and machine vision [3, 4]. Arrays of cantilevers for data storage could be combined with electronics to create a portable terabit storage device [5].

This research focuses on key technological building blocks for the development of a sensor system on a chip. Specifically, silicon electrical through-wafer interconnect (ETWI) technology is developed and integrated with a sensor array. The ETWI addresses key packaging and density issues associated with operating a sensor array. The sensor array, a two-dimensional array of silicon cantilevers, is a representative platform

that has broad sensing applications, as micromachined cantilevers are very sensitive and diverse sensors.

This chapter introduces microfabricated sensor arrays, with particular attention given to released sensors such as cantilevers. Electrical through-wafer interconnect applications in both IC and MEMS are then described. Next, the specific technologies used for fabricating ETWI are surveyed. In this discussion, several issues and challenges are raised, many of which will be addressed by this research. The focus of this work is then outlined: technology for silicon through-wafer electrical interconnects and released silicon sensors using anisotropic plasma etching.

1.1. Released Sensor Arrays

The term "micromachined sensor" generally refers to a thin film sensor that is fabricated with IC fabrication techniques. When the device is released, by removing the material beneath it, it can either deflect due to external forces and act as a sensor, or be driven to deflect and behave as an actuator. For example, membrane sensors can be used to make compact pressure sensors [6]. Released sensors can generate and sense acoustic radiation for use in proximity detection, thin film characterization, and ultrasound imaging [7, 8]. Tactile contact force measurements can be made with membranes to study the dynamics of insect locomotion and dexterous robotic manipulation [9].

1.1.1. Microcantilevers

In its most basic form, the microcantilever consists of a beam that deflects due to an external force. The force can be limited to interactions at a very sharp tip, providing planar resolution. The deflection can be measured with very high vertical resolution with a reflected laser beam to a nearby photodetector. An embedded stress sensor in the cantilever can also be used to detect deflection (Figure 1-1). When the probe and a sample are translated horizontally relative to each other, the sample topography can be mapped with atomic resolution. This scanning technique provides a powerful way to study surfaces at high resolution. Since its invention in the early 1980s [10], the atomic force microscope (AFM) has grown into a commercial microscope that typically measures piconewtons of force, with angstrom vertical resolution and nanometer horizontal resolution.

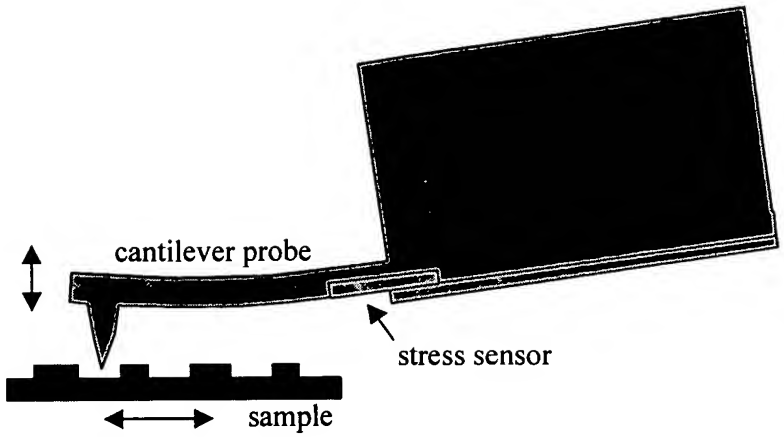


Figure 1-1. Schematic of a scanning probe cantilever with integrated deflection sensor. Arrows indicate direction of motion of probe and sample.

Cantilevers are an extremely popular sensor to work with because of their incredible sensitivity and versatility. The tip can be functionalized and in principle make measurements of magnetic, electrical, thermal, chemical, stress, and flow signals, with high sensitivity and speed [11]. Its ability to operate in water and at atmospheric pressures, unlike scanning electron microscopes (SEM), has lead to numerous biological imaging and force measurement applications [12]. Trace chemicals can be detected and identified with cantilevers that bend due to chemically induced stress [13]. In lithography, arguably the most critical technology for the integrated circuit industry, the scanning probe has demonstrated patterned lines as small as 300 Å wide, with a wider process latitude than electron beam techniques [14]. Functioning metal-oxide semiconductor transistors with 100 nm gate lengths have been demonstrated using scanning probe lithography [15]. Scanning probe devices using localized heating of a polymer can achieve 400 Gbits/in^2 data storage densities, an order of magnitude greater than demonstrated by magnetic techniques [16].

While the sensitivity of these techniques is most impressive, the throughput and sensing area are hindered by their reliance on serial scanning. For sample dimensions on the order of a micron or less, or when the sample is static and the time required to scan is not of concern, a single probe is generally adequate. However, commercial AFMs used for area imaging typically require on the order of ten minutes to image 100 μm × 100 μm

regions at the highest resolution. With parallelism the sample area can be increased and the scan time shortened.

1.1.2. Arrays

Arrays are generally important for microfabricated sensors because they increase throughput without sacrificing sensitivity. Cantilevers working in parallel have applications for both scanning and non-scanning applications.

For scanning applications, arrays increase sample area by summing the small areas scanned by each cantilever. If the sensitivity of each cantilever is maintained, arrays could enable cantilevers to lithographically pattern devices at nanometer resolutions across millimeter scale computer chips [17]. Important considerations include the speed and range of the scanner, and the density of the cantilevers. The scanner used to move the sample or cantilever array should not introduce vertical displacements larger than the signals being measured, which can be as small as a few angstroms. Such scanners typically have a range of only a couple hundred microns, making it important for the cantilevers to be densely packed. The faster the scanner can move (typically on the order of millimeters per second), the faster the array can scan over the entire sample. This form of lithography has the added benefit of not needing a separate mask, as this is a direct writing technique. Small, fabricated patterns also need to be imaged, so large area imaging of chips at very high-resolution would aid process monitoring. Combined with probe lithography, nanometer overlay could be achieved. For data storage applications, a thousand cantilevers working in parallel could make terabit storage drives possible [5].

Arrays also benefit applications where the probes do not scan relative to a sample. Many biological and chemical applications operate in a gas or liquid flow environment, which brings the sample close to the tips. The availability of multiple sensors provides options for variable functionality and redundancy. In chemical nose applications, each cantilever can be coated with a different chemical for specific chemical bindings. More cantilevers permit more chemical variations and more redundancy, which is important for chemical identification [13].

1.1.3. Cantilever Array Technology

Piezoresistive sensor arrays are attractive for array applications because they do not require cumbersome optics. Doped silicon can act as a very compact, integrated, and sensitive strain gauge, making the sensor an electrical device. Linear and two-dimensional arrays of piezoresistive cantilevers are being pursued by groups at Stanford, IBM and in Japan [5, 18-20] for applications in data storage and imaging, and will be described in detail in Chapter 4.

Key fabrication issues for cantilever array work include releasing and electrically connecting to each sensor. For cantilever arrays, the release process needs to be high-yield, uniform, and compatible with the other process steps. It is also important that the release process does not limit the packing density of the devices. Wet chemical etches from the backside of the wafer are commonly used for releasing devices but have limited aspect ratios and thus limited packing density. A high-density anisotropic dry release developed in this thesis addresses these issues, and will be discussed in Chapter 3.

Arrays of individually addressable devices require careful electrical wiring so as not to limit packing density. Combining other functions, in addition to displacement sensing, complicates the wiring challenge. Integrated actuators and sensors have already been fabricated, enabling constant force scanning over topography [18]. An integrated transistor for lithography control has also been fabricated on a cantilever [21]. An array of devices with all of these functions would enable lithography over topography on large areas, but would require multiple electrical connections per cantilever. Moving this wiring to the backside of the chip is an approach to this problem which will be introduced in the next section.

1.2. Motivations for Electrical Through-Wafer Interconnects (ETWI)

Electrical through-wafer interconnects (ETWI) have significant applications for integrated circuits (IC) and micro-electrical-mechanical systems (MEMS). The basic motivation is to move electrical device fabrication from two-dimensions to three-dimensions. Each application has its own geometrical, electrical, and material requirements.

1.2.1. Integrated Circuits Applications

Integrated circuits are primarily planar devices. Micron-scale thick layers are fabricated on substrates hundreds of microns thick. Modern ICs have many layers of wires, but not many layers of active devices. The ability to vertically stack chips with active devices would greatly increase density, speed and overall system integration ability. Optimized devices from incompatible materials processes can be brought together through packaging. Currently there are a variety of ways to combine chips into vertical multi-chip modules using peripheral wiring technologies, such as wire-bonding, tab connectors, or flex circuits. For the highest interconnection density, however, (where the interconnect sizes are on the order of the device), area interconnections with substrate through-wafer vias, as opposed to peripheral connections are desired [22, 23].

A high-density ETWI in the device substrate, when combined with wafer bonding or flip-chip technology, enables a multi-chip stack. If the ETWI are small (less than ten microns) and densely packed, they can transfer thousands of signals between stacked chips. Solid state memory chips that have high-density interconnects and low power requirements, are a particularly attractive application for this ETWI technology [24, 25]. Solder bumps and an intermediate ceramic carrier layer have been used to stack dynamic random access memory (DRAM) chips, but interconnects are limited to solder bump sizes (~100 μm) [26]. High-density vertical interconnects could bring together multiple layers of active circuits on device quality silicon and enable reduced interconnect delays and thus faster circuits [27]. For these IC applications, substrate vias with footprints and bonding alignment on the scale of current IC metallization lines (less than 1 μm) are desired. A metal such as copper would be used for metallization because these memory chips are generally high-speed applications with frequencies in the gigahertz range.

Substrate ETWI greater than ten microns also have important IC applications. ETWI, in conjunction with the appropriate bonding technology, could be used to connect global signal lines between chips, which may require lower density. Examples include connections for integrated passive components for radio frequency (RF) circuits. If inductors, capacitors, and resistors, which are currently off-chip, could be integrated onto a single chip, cell phone sizes could be reduced from printed circuit board dimensions to chip scale dimensions (millimeter scale) [28-30]. Low loss substrates such as glass could

be used for the passives and connected to silicon or gallium arsenide-based transceiver circuits. Larger ETWI could also provide ground and power between chips or between a single chip to its package. A low impedance substrate via connection to a backside ground is an important way to reduce parasitics in RF circuits [31, 32]. Such a ground connection can also be used to protect sensitive analog sections of a mixed signal chip from noisy digital circuits with a Faraday cage [31]. Very low impedance (less than 1 Ω) connections are generally required for RF and power supply applications.

1.2.2. MEMS Applications

In addition to aiding in numerous IC applications, ETWI are important because they provide three-dimensional design flexibility. MEMS sensors generally interact with the environment, which may or may not be compatible with electrical connections and standard IC chip packages. For a single chip application, ETWI can move bond wires from the sensor side of the chip to the back. For devices that require close proximity to a sample, such as proximal probe sensors, sensor-side wire bonds that are hundreds of microns tall dramatically restrict available sensing geometry. In the case of an array of scanning probe cantilevers, which need to be within a few microns of the sample or closer, this restricts the sample size to the size of the chip (Figure 1-2). For sensors that interact with a corrosive or electrically conducting environment, ETWI efficiently protect the electrical signals without having to embed wire-bonds in protective adhesives. Examples include underwater ultrasound imaging arrays and cantilever sensors for biochemical applications such as genetic diagnostics [33, 34].

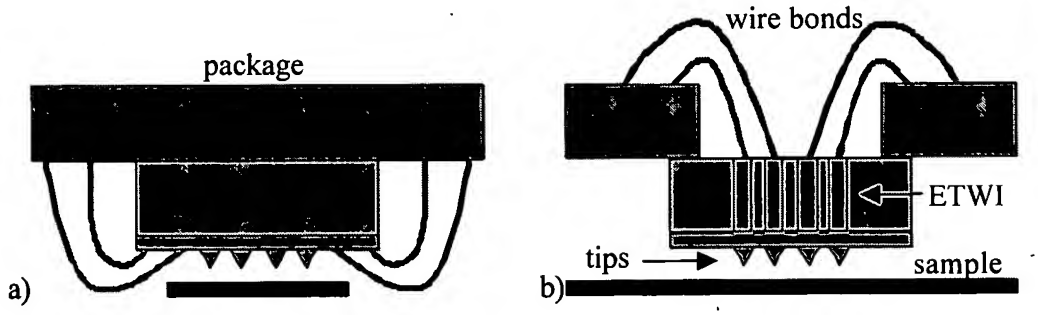


Figure 1-2. a) Wire-bonds on the sensor side of the device can obstruct proximity sensing and complicate liquid use. b) ETWI move wire-bonds away from the sensor, enabling proximity sensing over large samples and electrical protection from wet environments.

For sensor arrays which need to be high-density, ETWI serve to move electrical wiring away from the sensor side to allow for higher fill factors. Regions without sensors that are instead occupied by wires contribute to dead space which reduces imaging quality for membrane based sensors such as ultrasound transducers, pressure sensors, and force plate detection arrays. Wiring can quickly consume a large amount of chip area, especially when multiple electrical interconnects are required for each device. As sensors and actuators continue to be integrated, the need for electrical connections increases. Another example with individually addressable connections is a scanning probe array with integrated actuators, sensors, and transistors for large area imaging and lithography, previously described in Section 1.1.3. Such a system would require three electrical connections and a ground for each cantilever. To use ETWI in this application, its footprint size should be much smaller than the cantilever so as not to limit packing density. The ETWI resistance should be significantly smaller than the devices. In the case of piezoresistive cantilever sensors, an ETWI with a 30 μm diameter footprint and a resistance less than ten ohms meets these criteria. A two-dimensional piezoresistive cantilever with integrated ETWI for large area imaging is demonstrated in this thesis and will be described in Chapter 4.

Other MEMS applications for ETWI include structures where the ETWI is not simply a connection wire, but part of the device. Previous researchers have used ETWI to fabricate three-dimensional coil inductors for RF applications requiring a high quality factor [35]. ETWI have also been used to create through-wafer diodes for solid state detectors for high energy physics experiments [36].

1.2.3. Integrating MEMS and ICs

Integration of MEMS and ICs is one of the most important opportunities for realizing fully integrated systems capable of sensing, processing, storing and communicating information. Electrical circuits for sensors, such as amplifiers and analog to digital converters, should be placed close to sensors for optimal noise and speed performance. For actuators, power amplifiers and control systems are critical functions that can be provided by nearby electronics.

One approach to the integration of MEMS and ICs is to combine fabrication processes onto the same substrate. Typically the sensors and actuators are fabricated after the circuits, which is usually CMOS based. Examples of this approach for released devices include micromachined accelerometers, pressure and flow sensors [37]. Controlling the stress of the CMOS process thin films, which are to have structural functions in the MEMS devices, is particularly important and challenging [38, 39]. Because it is very difficult to alter the IC processing to accommodate the MEMS, usually the MEMS process is altered to accommodate the IC process. This means the MEMS process must be low temperature compatible (less than 400°C), so as not to disturb the metal IC lines. Released MEMS structures with tall protruding structures such as tips are difficult to fabricate because the integrated circuits already define the highest silicon substrate layer. MEMS processes which require high-temperature steps, such as thermal oxidation to sharpen tips and annealing to control piezoresistor doping profiles, need to be avoided or compromised to be integrated with the IC process. MEMS fabrication processes which involve chemicals and materials that are not generally IC compatible, such as sodium based etchants, are also restricted. In general, the optimal design for the MEMS device, and thus the overall system, is compromised to achieve integration.

Multiple chip modules (MCM) provide an alternative solution. This approach allows chips from separate optimized processes and different materials systems to be brought together through packaging [40]. From a testing point of view, this permits known-good-die to be determined prior to system integration, potentially reducing manufacturing costs. Ceramic chips with patterned metal lines are currently being used by the IC industry to place multiple chips in a single package and electrically connect them [22]. The chips can be either wire-bonded or flip-chip bonded to the ceramic substrate. Commercial MCM manufacturing techniques can also been used to combine MEMS and ICs. It has been found that an isotropic silicon dry release process using XeF_2 could be implemented after MCM packaging [41]. A major challenge for MCM technology is the inductance of the interconnect, because for high-frequency applications the wire-bonds are not ideal wires. In addition, MCM technologies are still essentially planar packaging technologies that do not reach the packing density possible with 3D chip stacking. It is possible to place one chip on another, but the size of the top chip

needs to be smaller than the bottom chip to allow for wire-bonding, and the stack is limited to two chips.

A packaging technology with higher interconnect and overall packaging density is possible when bonding is combined with ETWI, as area, instead of just periphery, bonding can then be used on multiple chips. Control and signal conditioning electronics could be placed close to the sensors, enhancing performance and immunity to noise. The MEMS process can be optimized separately from the IC process. A group at Stanford is using ETWI to combine released ultrasound transducers with a separate signal processing chip (see Chapter 6) [33]. Wafer scale bonding could be used to package many sensors at once, though with the same known-good-die concerns mentioned above. Thermal issues could be addressed by integrated micro-channels with pumped coolant [42]. Compact fully integrated systems, with multiple wafer stacks of sensors and electronics, would be possible (Figure 1-3).

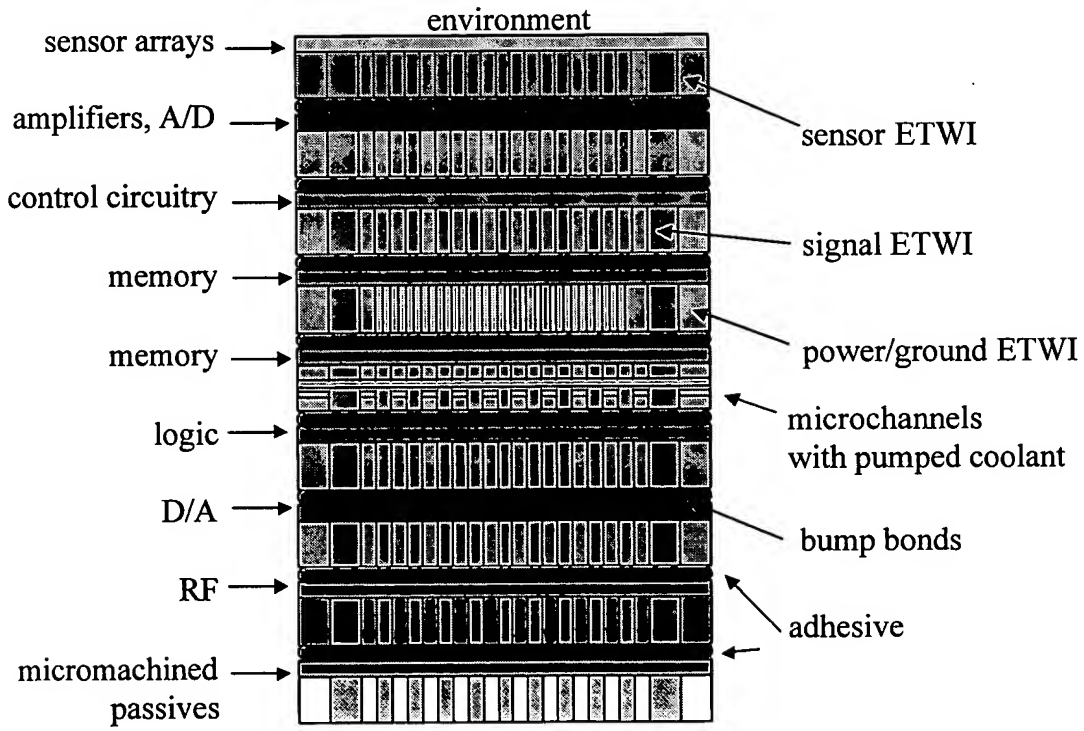


Figure 1-3. Schematic of various electrical through-wafer interconnect applications combined to form a smart wireless transducer.

Major challenges to realizing such systems are the bonding technology and the ETWI. The ideal bonding technology would be low temperature so as not to disturb the devices, and would likely be combined with a bump bond technology, similar to the previously described 3D memory stacks [26]. The size and pitch of the bonds must be coordinated with the ETWI. These depend on the specific fabrication technology of the ETWI, which will be discussed next.

1.3. Silicon ETWI Technology

The ideal ETWI technology, for the majority of applications described above, would have the smallest footprint possible and would electrically approximate an ideal wire: zero resistance, capacitance and inductance. However, the physical proximity of the substrate and other devices, combined with the limits of fabrication technology, force designers to compromise and build ETWI that are limited to the specifications for the particular application. The essential steps for forming ETWI in a substrate are 1) form the via, 2) deposit an isolation layer, and 3) deposit a conducting layer. The process technology is intimately connected to the substrate material, primarily through the etching technology. Though ETWI are being pursued in other materials such as glass and gallium arsenide [4, 32, 43-46], this review focuses on silicon. Silicon through-wafer etching technology will be reviewed in detail in Chapter 2. Active isolation technologies, such as reversed p-n junctions, are also possible [36, 47], but passive isolation is generally easier to implement and will be the focus of this survey. The conduction layer needs to be deposited conformally and provide enough conductivity for the application. Important integration issues include the temperature of the process and the way the layers are to be patterned.

ETWI technology can be classified as having either large or small footprints, low or high density, and post-process or pre-process. The footprint refers to the via diameter on the topside (device side), of the wafer. Density refers to how many isolated electrical interconnects can be packed into a given area. Post-process is defined as low-temperature and compatible with fabrication on a wafer that already has CMOS. Pre-process refers to an ETWI that is fabricated prior to MEMS or CMOS fabrication.

1.3.1. Large Footprint

A variety of processes have been used to fabricate ETWI with footprint diameters of hundreds of microns. One approach uses a wet silicon etch, followed by thermal oxidation for isolation, and metal evaporation (Figure 1-4a). ETWI with approximatelh 10 Ω resistance and 1 pF of capacitance have been demonstrated. Patterning the metal over the topography of the unfilled via required the use of an unconventional lithography process based on electro-deposited photoresist [48, 49]. It is possible to achieve isolated wiring densities of approximately 40/mm^2 by developing lithography capabilities inside the side-walls of the via, but the vias must be spaced by hundreds of microns, making the overall density much less. Using a bonded or integrated shadow mask to deposit the metal is another approach, which can also pattern lines in holes [50]. Because high-temperature oxidation and nitride were used in these approaches, CMOS circuitry could not be fabricated before the ETWI. However, a low-temperature isolation layer could be used instead, making the process a possible add-on module, which could follow CMOS fabrication. Despite the via being unfilled, these technologies were able to perform lithography on both sides of the substrate.

Recently, isotropic silicon plasma etching has been used to form ETWI in silicon. This process uses a low-temperature oxide and metal followed by filling with polyimide [51]. The footprint of the via was 200 μm in diameter, but the process was combined with wafer thinning so that the original etch did not have to go through the entire thickness of the substrate. For wafer stacking applications, this work achieves an important task, which is to expose an isolated connection on the backside of the wafer for bonding without needing to perform backside lithography. However the footprint is large and the density is low (2/mm^2). Combining this work with an anisotropic etch process to achieve higher densities is a promising approach for high-density post-process ETWI fabrication.

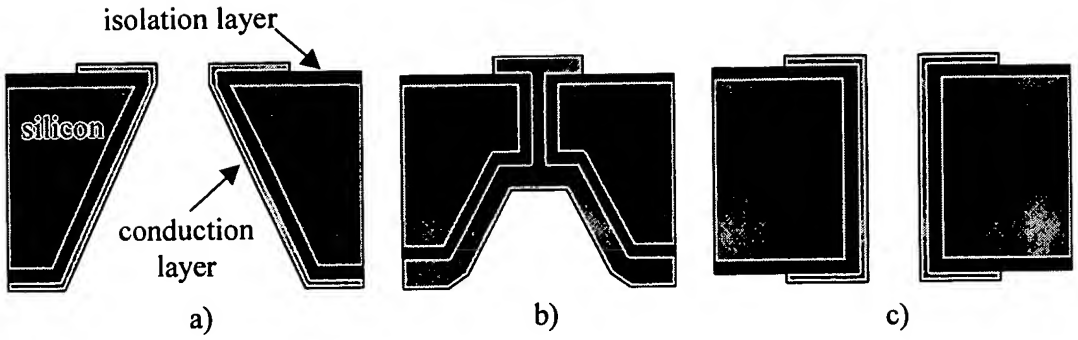


Figure 1-4. Drawing of various ETWI fabrication technologies. a) wet etch, b) wet etch and anisotopric etch, c) anisotropic etch.

The bulk silicon substrate has also been used as a conductor [52]. Trenches were etched around a section of low-resistivity (0.01 Ω-cm) silicon substrate hundreds of microns wide. The trenches were filled with tetraethoxysilane as a low-temperature isolation layer. This process is low-temperature, but requires polishing and forms ETWI with a resistance of a few kilo-ohms, too high for many applications described above.

1.3.2. Small Footprint

Many groups are pursuing processes for ETWI with footprints on the order of ten microns. A combination of wet etching and anisotropic etching can be used to form vias 10 μm in diameter on the top-surface [31, 53]. However, the use of wet etching leaves vias hundreds of microns wide on the backside, which restricts the packing density to less than 5/mm^2 (Figure 1-4b). This etching can be followed by low temperature (less than 400°C) plasma enhanced chemical vapor deposition of nitride and then electroplating of metal through the small via. Low resistance (less than 1 Ω) and inductance (200 pH) has been demonstrated with this post-process ETWI for RF applications [31]. Because of the deep trenches on the backside, lithography is only performed on the frontside (device side) of the wafer.

Recent advancements in plasma etching enable anisotropic etching through the entire substrate to form ETWI tens of microns in diameter with densities greater than 400/mm^2 (Figure 1-4c). Thirty-micron diameter vias have been etched through a 500 μm thick silicon wafer and thermally oxidized and electroplated with copper to form ultra-

low resistance ETWI for RF applications [35]. The vias were unfilled, so electroplated lithography was used to pattern the ETWI on both sides of the wafer.

Two ETWI demonstrations that did not have passive isolation layers also deserve mention. Both used substrate thinning to shorten the distance required for the via etch. The silicon wafers were thinned to 200 μm and then mounted on sacrificial substrates to be removed later. For an RF application, one group etched 60 μm diameter vias and then electroplated with gold; high resistance substrate silicon was used for isolation [54]. To form 3D electrodes, another group etched 20 μm diameter vias through the thinned substrate, and then filled the vias with doped polysilicon [36]. The vias were not isolated, and lithography was only performed on one side of the wafer so the vias were not individually characterized. Thinning the wafer to simplify etching requirements is an attractive approach, as higher aspect ratio holes, and thus small footprints and higher densities can be achieved. However, thin wafers are often too delicate to handle in standard semiconductor processing equipment and thus need a carrier wafer, meaning they cannot be processed on both sides.

1.3.3. Pre-Process for Released MEMS

To use an ETWI in a device requires integration of the ETWI process with the device process. The aforementioned ETWI processes that used only low temperature processes were classified as post-processes, e.g. they could possibly follow a CMOS process. The processes generally could pattern the metal only on one side of the wafer, unless exotic techniques such as electroplated resist or shadow-masking was used. For ETWI that are to be integrated with an IC, the post-process approach is attractive because it avoids complicating the IC process. IC processes based on foundry facilities generally have very rigid fabrication parameters and limited materials. However, for integration with released MEMS sensors, such as cantilever arrays, a post-process with lithography is very difficult to perform after the structures are freed from the substrate. They are compliant and fragile, and generally cannot be easily masked with photoresist. Consequently, the release step tends to be the final process step in a MEMS process.

To integrate ETWI with released MEMS structures this work proposes using pre-processed ETWI. The ETWI is first fabricated using high-temperature compatible

materials, such as polysilicon or tungsten. An anisotropic via (20-30 μm diameter) is etched through the entire wafer to enable a footprint size that does not restrict device packing density. Then the MEMS process is performed on the wafer, after ETWI fabrication, enabling lithography on both sides of the wafer.

1.4. Thesis Summary

This thesis addresses the multiple challenges described above by developing technology for pre-processed electrical through-wafer interconnects and for released sensor arrays.

The recently developed time multiplexed inductively coupled plasma (TMICP) etching process is a key technology for this work, as it enables the dry etching of very high-aspect ratio holes in silicon wafers. Stanford was fortunate to obtain one of the first commercially available tools with this process, but with virtually no characterization data. Chapter 2 describes the TMICP process and experiments performed to measure important characteristics of the new process, with emphasis on features relevant to through-wafer etching.

In Chapter 3, the TMICP process is applied to the general problem of releasing high-density structures from the backside. The specific case of a two-dimensional array of cantilevers is demonstrated. Techniques developed to accurately release structures and handle wafers for through-wafer etches are described.

In Chapter 4, this release process is combined with an electrical through-wafer interconnect (ETWI) and high-aspect ratio tips to form a two-dimensional array of piezoresistive cantilevers. The ETWI are fabricated prior to the cantilever fabrication to facilitate integration. The cantilevers and interconnects are fabricated, characterized, and successfully used to perform parallel contact mode scanning microscopy. However, the ETWI, based on tungsten through a 30 μm hole, were unfilled, which complicated masking of long etches and reduced yields.

An improved ETWI based on an isolated polysilicon plug is described and characterized in Chapter 5. This device is integratable with MEMS, and possibly IC processes, as it uses high-temperature compatible materials and standard lithography. N-

type, p-type and shielded ETWI versions are all fabricated, characterized and modeled to extract the electrical properties of a single interconnect.

Finally, Chapter 6 addresses current work to integrate the polysilicon filled ETWI with two types of ultrasound sensors. The capacitive based ultrasound transducer is a project in Professor Khuri-Yakub's group at Stanford, and the ETWI integration is led by Ching Cheng. Venkataraman Chandrasekaran is developing the piezoresistive acoustic sensor as part of his work in Professor Mark Sheplak's group at the University of Florida. The p-type polysilicon ETWI were developed in conjunction with this project.

In summary, the main contributions of this work are:

- *A novel technique for the accurate anisotropic backside dry release of free high-density structures.*
- *Demonstration of a novel 2D array of piezoresistive scanning probe cantilevers with integrated tungsten electrical through-wafer interconnects for large area imaging.*
- *Demonstration of a novel polysilicon-filled, passively isolated, electrical through-wafer interconnect, with n-type, p-type and shielded variations. Integration with released MEMS processes is demonstrated and integration with IC processes is possible.*

Chapter 2: Deep Silicon Etching

A key technology for the fabrication of electrical through-wafer interconnects is deep silicon plasma etching. This chapter reviews traditional silicon etching techniques and explains their limitations for through-wafer etching. The characterization of a new commercial etching process (TMICP), capable of deeper and higher-aspect ratio etching, is presented. Finally, deep etch design implications of this study are given.

2.1. Evaluation Of Deep Silicon Etching Techniques

Traditional anisotropic silicon etching is done in either a bath of wet chemicals, or in a dry reactive ion etcher [55]. Both approaches have well characterized etch rates and standard masks, however, both have severe limitations when a deep, anisotropic high-aspect ratio hole is required. Here anisotropy refers to how close the etch profile is to being normal to the surface. A very anisotropic etch is perpendicular to the surface throughout the depth of the etched hole. A vertical via can be described by its aspect ratio (AR), which is defined as the final etched depth divided by the minimum feature size of the hole at the surface.

2.1.1. Wet Etching

Examples of wet etching applied to ETWI were given in Section 1.3. Commonly used silicon wet silicon etches include ethylene diamine pyrocatechol (EDP), potassium hydroxide (KOH), and tetramethylammoniumhydroxide (TMAH). Deep etches that are hundreds of microns deep can be masked with silicon dioxide (SiO_2) or silicon nitride

(Si_3N_4), as photoresist masks do not perform well in these etchants. However, chemically driven etches have crystal plane dependent etch rates which result in preferred etching along a 54.7° angle for (100) oriented silicon wafers. This inherently limits the anisotropy and aspect ratio of the etch. However, very smooth sidewalls (optical scale roughness) can be produced with wet etching.

2.1.2. Porous Silicon

Silicon can be converted to porous silicon in the presence of concentrated hydrofluoric acid (HF) when the back of the wafer is illuminated to generate holes and a bias is applied [56, 57]. By starting with micropits in the silicon etched by KOH, porous silicon etching can etch 1-10 μm diameter holes anisotropically hundreds of microns deep [58, 59]. Such aspect ratios (~250:1) and depths are significantly better than conventional wet etching and reactive ion etching techniques. However, masking is very cumbersome as Si_3N_4 and silicon carbide (SiC) is required on the HF side of the wafer, and aluminum on the backside. These masking requirements tend to restrict process flexibility because they incur metal contamination and deposition, and etching of SiC is not standard. Despite these challenges, porous silicon produces unprecedented aspect ratios and holds promise as a future through-wafer etching technique.

2.1.3. Reactive Ion Plasma Etching

Plasmas are neutral gases of ions, free electrons, and free radicals. Free radicals are neutral species with incomplete bonding, making them very chemically reactive. For example, the free radicals fluorine and CF_3 both react with silicon to create a volatile product, chemically etching away silicon. Ions driven by a bias can physically sputter silicon atoms away by striking atoms on the surface and physically dislodging them. If the ions are driven normal to the surface they can etch with high anisotropy. Ion bombardment can also enhance chemical etching due to free radicals.

Conventional silicon plasma etching is performed with single electrode parallel plate reactive ion etchers. One electrode is used to both generate the plasma and drive the ions. Increasing the power of the electrode increases the plasma density and ion power and thus increases the silicon etch rate and profile anisotropy, but at the expense of the photoresist etch rate. Etch selectivity is the ratio of the etch rates between the

material to be etched and the mask. The etching selectivity of silicon to photoresist is limited to 10:1 and the profiles are only slightly anisotropic. Using 20 μm of photoresist, aspect ratios are limited to approximately 2:1, with depths up to 100 μm.

Newer anisotropic plasma etchers generate high-density plasmas at lower pressures (HDLP) than single electrode machines. By using two electrodes, the top one to generate the plasma and one the bottom one to drive the ions, they are able to increase the silicon etch rate by using higher ion density plasmas, instead of by increasing the ion driving power. Microwave electron cyclotron resonance and inductive coupling are two techniques commonly used to generate plasmas with ion densities greater than 10^{11} cm^{-3}, which are orders of magnitude greater than single electrode sources. The increased number of ions and free radicals increases the etch rate, without significant increases in ion power. This avoids increases in mask sputtering which reduces mask selectivity. HDLP etchers operate at a low pressure, on the order of 10 millitorr, which helps to increase the directionality of the ions.

Sidewall passivation is combined with HDLP etches to reduce lateral etching and increase etch anisotropy. Oxygen, hydrogen, and carbon are used to form SiO_x from reactant byproducts that continually coat the etched trench sidewalls and base as the silicon etch progresses (x is a variable integer). The SiO_x passivation is preferentially etched in the base because of the ion directionality, increasing anisotropy. This technique is used with common silicon etchants such as fluorine, chlorine or bromine based chemistries. The result is increased anisotropy (AR ~ 8:1) with reasonable mask selectivity (3:1 for photoresist and greater than 10:1 for silicon dioxide). While this etching process is very popular for many integrated circuit applications such as dynamic random access memory (DRAM) capacitor trenches, the etch rates (~3000 Å/min) and the maximum depths (20–40 μm) are inadequate for through-wafer etches.

Reducing the surface temperature of the wafer can increase the effectiveness of the sidewall passivation. Reduced temperature reduces the volatility of the silicon reaction byproducts, reducing chemically driven lateral etch rates. Cryogenic temperatures of −100°C to −130°C have been used to achieve an increased etch rate of greater than 2.5 μm/min, an oxide mask selectivity of more than 100:1, and an AR of up to 15:1. Depths of up to 100 μm have been achieved. Unfortunately, cryogenically

cooling the wafer is costly, often plagued by condensation problems on the wafer, and does not permit standard photoresist masking.

2.1.4. Time Multiplexed Inductive Plasma Etch Process

The deep silicon etching technique which we consider most appropriate for high-aspect ratio anisotropic through-wafer silicon etching is an HDLP process with an inductively coupled plasma source and a time-multiplexed switched gas scheme for passivation. The technique was invented by Bosch [60] in 1994 and has since been commercialized by Surface Technology Systems (STS) and Plasma-Therm for applications in silicon micromachining. Stanford University obtained one of the first prototype tools from STS in 1995 and demonstrated some of the first MEMS devices using the deep silicon etch [61]. Very little characterization data was available for the machine, so in 1997 we began exploring the ability of the process to achieve very deep to through-wafer etching.

The time-multiplexed inductively coupled plasma (TMICP) etching process permits very deep (hundreds of microns) high-aspect ratio holes (AR ~ 40:1) to be etched in silicon with only 20 μm of photoresist. Similar to standard high-density low-pressure plasma etchers, separate top and bottom electrodes enable high etch rates and increased anisotropy. However, significantly higher aspect ratios are achieved by using a time multiplexed process which continuously switches between passivation and etching steps. A fluorinated gas (SF_6) is used to etch the silicon (Figure 2-1b), with a high top power for high etch rates (greater than 600 W) and low bottom power (10 W) to maintain high silicon to resist selectivity (60:1). After a few seconds, SF_6 is pumped out of the chamber and C_4F_8 pumped in. A thin teflon like passivation layer is deposited on the wafer, including the base and sidewalls of the previously etched hole (Figure 2-1c). Then SF_6 is pumped in again. The fluorine radicals are able to break through the passivation more readily if they are ion-assisted. Since the bottom power drives ions vertically, the side-walls are not bombarded directly, while the base of the hole is. Hence the passivation is removed from the bottom of the hole first, and the fluorine attacks the silicon there (Figure 2-1d). This continued switching between passivation and etching permits increased anisotropy (~90° throughout the hole) with high etch rates (1-5 μm/min).

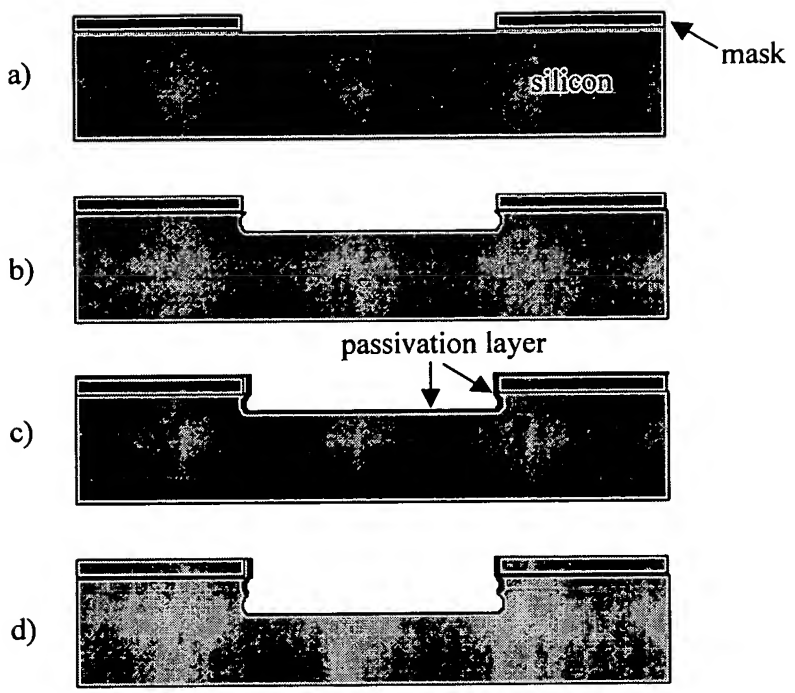


Figure 2-1. TMICP process. a) Silicon wafer with patterned mask. b) Etch cycle. c) Passivation cycle. d) Etch cycle preferentially attacks the bottom of the via.

2.2. TMICP Characterization Experiment

The initial goal of the characterization experiment was to determine which process conditions and wafer handling techniques were most appropriate for through-wafer etching. However, characterization data for Stanford's machine was very minimal so a broader characterization was undertaken. Etch rates, profiles, and mask selectivities were characterized for three standard process recipes. Etch lag, where different size holes etch at different rates, is a known characteristic of reactive ion etching which needed characterization for TMICP for a variety of applications. Uniformity across the wafer and the effect of pattern density were also examined.

The starting substrates were 4-inch diameter single-sided p-type wafers, with 10-20 Ω-cm resistivity and 475-575 μm thickness. After scribing the wafers, standard 1 μm photoresist lithography was used to pattern a label mask into the silicon to aid in identification of the test structures. These labels were transferred to the silicon by plasma etching.

For the deep etch mask, photoresist was selected over thermal oxide for simplicity and integration flexibility. While thermal oxide is known to have higher silicon selectivity (~150:1), Stanford had just obtained access to a new photoresist capable of 5-20 μm thick deposition (Shipley AZ4620). Photoresist selectivity was expected to be about half that of oxide, but patterning was expected to be much simpler and many fabrication processes are not compatible with the high-temperatures required for oxide deposition. An 8 μm photoresist lithography process was developed to optimize the sidewall performance. The labeled wafers were singed for 30 minutes at 150°C, coated with hexamethyldisilazane (HMDS), and then coated with photoresist at 2400 rpm for 60 seconds. After baking for 60 min at 90°C, the test pattern was exposed in a 1:1 projection lithography stepper (Ultratech Model 1000) with 1350 mJ of ultraviolet light and developed (Shipley AZ400K). The resulting profile control is depicted in Figure 2-2.

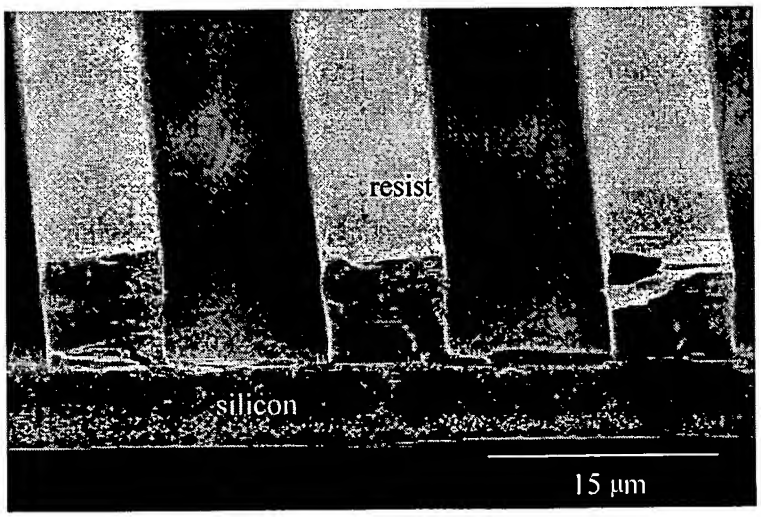


Figure 2-2. Thick photoresist profile after exposure and development.

Test structures for each die consisted of squares (L × L), rectangles (L × 200 μm), and trenches (L × 2000 μm), where L varied from 2 μm to 200 μm. These shapes covered the size range typical of most deep etching applications and were intended for measurements of aspect ratio dependent etching. To measure the effect of loading, two pattern densities (5% and 15% of the wafer) were created with the same die, varying the repetition of the die pattern. The single die of test structures was drawn to maintain a

constant local density over each region (squares, rectangles or trenches) in an attempt to subject each hole to the same local loading. Structures were staggered to aid in obtaining representative cross-sectional slices through the wafer.

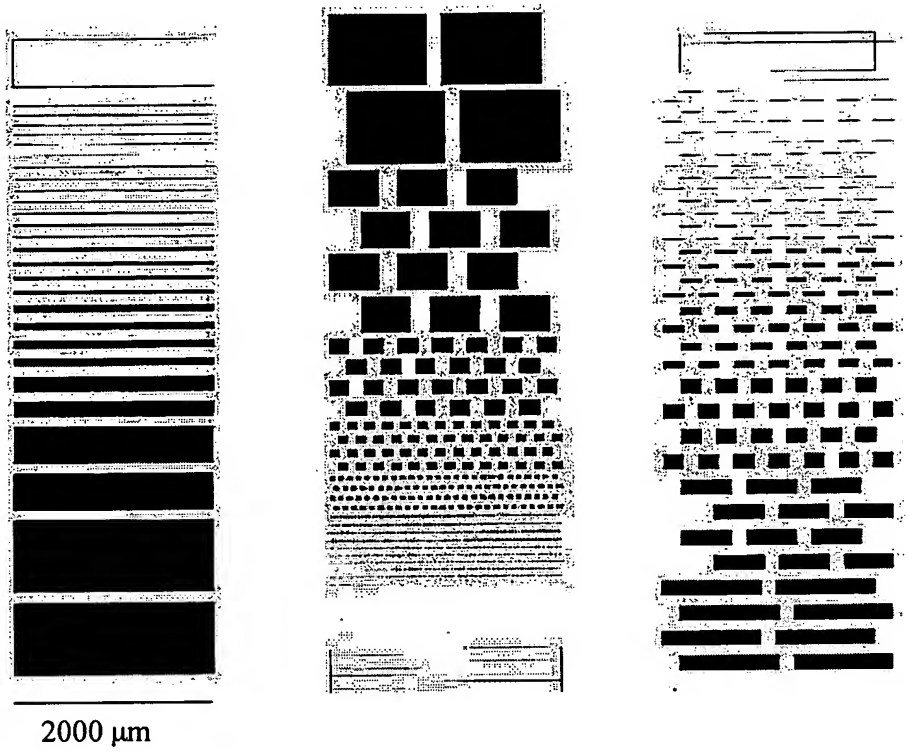


Figure 2-3. Mask pattern of etch test structures.

Previously developed, but uncharacterized, recipes were provided by the TMICP manufacturer (STS). These recipes had each been tuned for anisotropy with varying balances between etch rate and sidewall smoothness. A summary of the etch recipes is given in Table 2-1. Automatic pressure control (APC) refers to the angle of a valve that is fixed, allowing the chamber pressure to be set by the gas flow rate. The backside cooling of the wafer was kept constant by maintaining the helium pressure at 9.7 torr under the electrostatic chuck.

Etch Recipe	DEEP	SMOODEEP	SMOOSHALL
SF_6 flow rate [sccm]	130	130	130
SF_6 active time [sec]	11	8	7
Etch electrode power [W]	12	8	12
C_4F_8 flow rate [sccm]	85	85	120
C_4F_8 active time [sec]	8	6	7
Passivate electrode power [W]	0	0	0
Coil power [W]	600	600	600
APC angle [°]	70	70	55

Table 2-1. Parameters of STS Etch recipes.

Etches were performed for 5, 20, 40 and 80 min for each of the three recipes. The resulting depths ranged from a few microns to 400 μm. Resist etch rates were monitored using a thin film spectro-reflectometry measurement tool (Nanometrics). A wafer saw (Kulicke & Soffa) was used to cut through the entire wafer, using a slow blade feed rate (2.5 mm/sec) to minimize cross section damage. Photoresist was later stripped with acetone to avoid excessive charging during scanning electron microscope (Hitachi S-800) measurements of the cross-sections. Depth measurements were referenced to the center of the hole base and multiple measurements were made in the center of the wafer and along the edge of the wafer for each test structure. Typical cross sections are given in Figure 2-4.

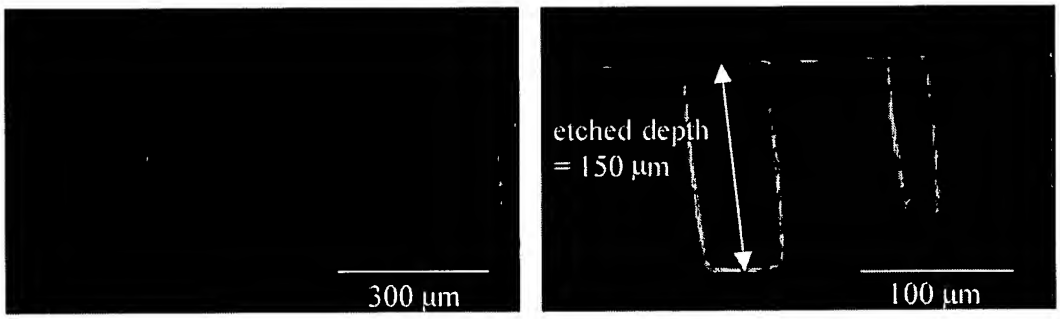


Figure 2-4. SEM cross section of typical TMICP etch test samples.

2.3. Characterization Results

Three main characteristics of the etches were studied: rate, profile, and side wall integrity. Results for the longest etch time, 80 min, are summarized here, as the longer etches most clearly demonstrate the trends. The complete set of characterization results is presented in Appendix A.

2.3.1. Etch Rate Dependencies

The hole size was found to have a strong effect on etch rate. Figure 2-5 shows how etch rates can be reduced by as much as a factor of 2 when the hole dimension L is reduced by a factor of 10. The effect is more pronounced for squares than trenches and rectangles. For holes with $L > 100$ μm, a plateau is observed. Figure 2-6 depicts the time evolution of the etch depths, and shows how the slope of the data for $L < 100$ μm grows steeper with time. The etch rate is shown to decrease as the etch proceeds, as the average etch rate for $L = 10$ μm is 5 μm/min for the first 5 min, but 2.1 μm/min for the last 60 min. The phenomenon of the etch rate depending on the size and depth of the via is common to fluorine based plasma etches and called aspect ratio dependent etching (ARDE) [62]. The specific mechanisms involved are under study by other research groups, but are generally attributed to increased transport of reactants to the bottom of the via and increased transport of etch products out of the via as the diameter increases and the depth decreases [63].

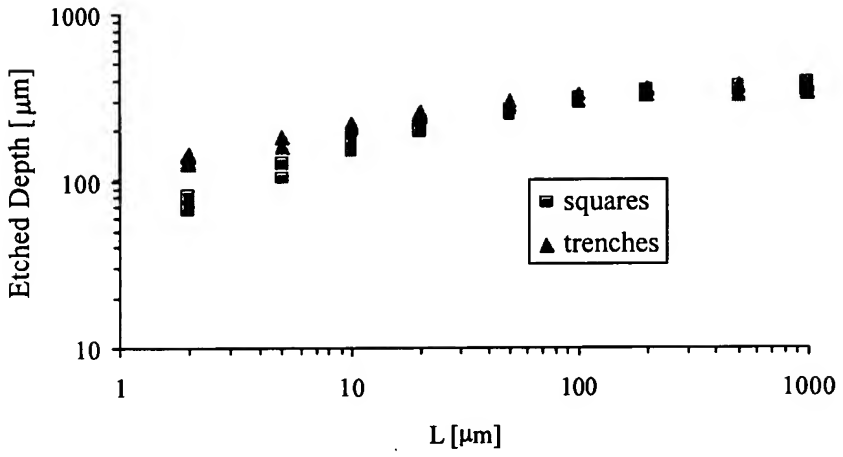


Figure 2-5. Etch depth dependency on hole size for 80 min etching of program DEEP of squares of side L and trenches of L × 2000 μm.

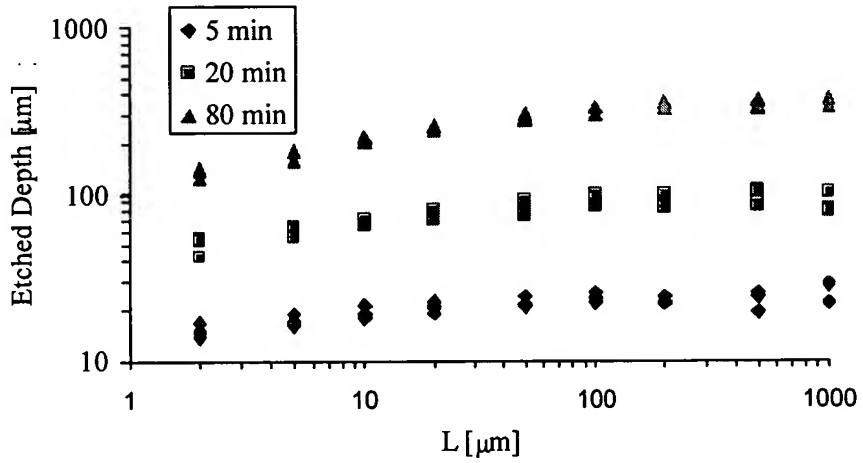


Figure 2-6. Etch lag dependency on etch time for recipe DEEP and trenches L × 2000 μm.

The three etch recipes had a wide range of etch rates, with SMOOSHALL being the slowest (Figure 2-7). All recipes demonstrated significant lag for L < 100 μm. The high etch rate of recipe DEEP can be explained by the long SF_6 active time and the high SF_6 electrode power. The side wall smoothness was not studied here, but SMOODEEP is expected to have smoother side walls then DEEP because the cycle times are shorter. The scalloping nature of this process (Figure 2-1) can be reduced when the switching frequency between etching and passivation is increased. Recipe SMOOSHALL works in a lower pressure regime and is designed for shallower etches with smoother side walls. It was observed to have reduced selectivity between silicon and photoresist etch rates (Table 2-2).

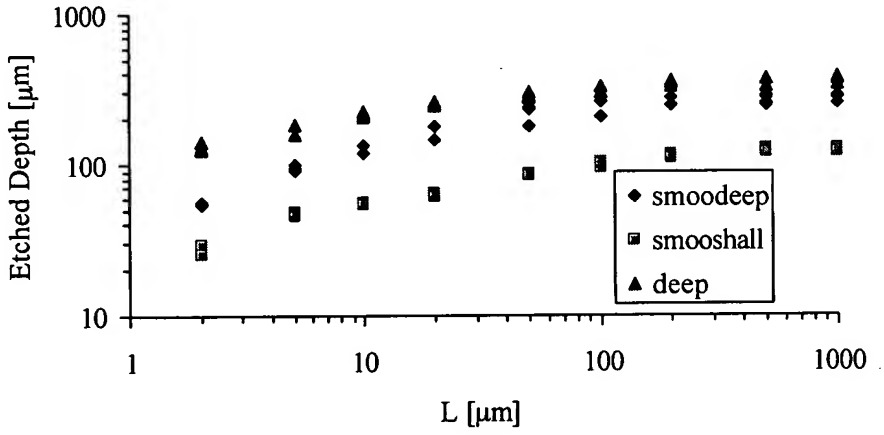


Figure 2-7. Etch depth dependency on recipe for 80 min etching of squares of side L.

	Etch Rate		Selectivity
Etch Recipe	**Silicon [μm/min]**	**Photoresist [Å/min]**	**Silicon/Photoresist**
DEEP	3.8	370	103
SMOODEEP	2.9	239	123
SMOOSHALL	1.2	288	42

Table 2-2. Etch rate summary for standard TMICP etches based on 80 minute etches.

Non-uniformity of the etch depth across the wafer was significant, as etch rates along the edge of the wafer were 5-15% faster than rates in the middle of the wafer. This variation was maximum when the exposure density, defined as the fraction of the entire wafer surface not masked, was increased from 5% to 15%. The increase in exposure was also observed to slightly reduce etch rates (Figure 2-8), suggesting the amount of available of reactants was insufficient for the amount of silicon being etched.

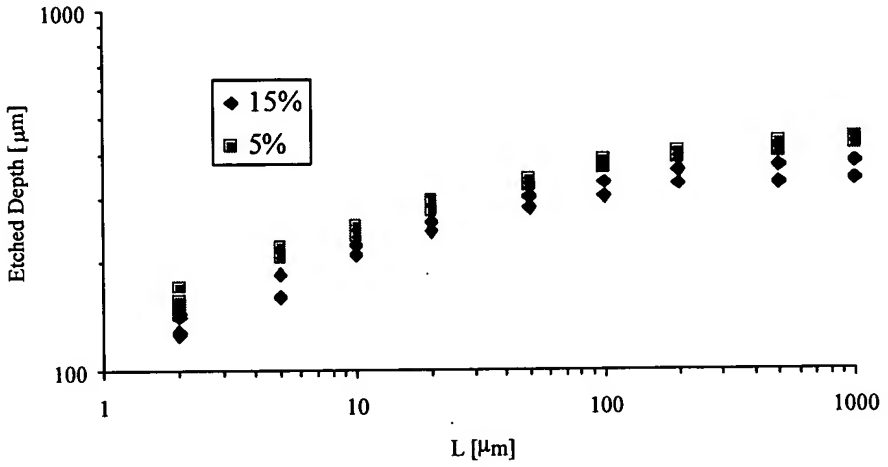


Figure 2-8. Etch lag and uniformity as a function of pattern exposure density for 80 min of recipe DEEP for trenches L × 2000 μm.

2.3.2. Etch Profile

Vertical profiles (~90°) with relatively flat bottoms (depth variation of less than 2%) were observed for L > 100 μm. However, as L decreased, particularly less than 10 μm, V-shaped profiles (depth variation greater than 25%) became apparent. Resist mask erosion occurs when the resist along the edge of the pattern etches quickly and recedes. This widens the silicon hole, and can have a profound effect when L is on the order of the resist thickness or smaller. Because of this, reported etch depths for L < 10 μm may be larger than they would be if a hard mask (oxide or metal) were used. Figure 2-9 shows a box-shaped and V-shaped profile from the same etched wafer. Recipe DEEP generally had a more box-like profile than SMOODEEP, as depicted in Figure 2-10. Other groups have also reported increased anisotropy when a higher etch electrode power is used (DEEP used 12 W and SMOODEEP used 8 W) [62]. However, increasing the bottom

electrode power also increases ion sputtering of the mask, and thus reduces mask selectivity (see Table 2-2).

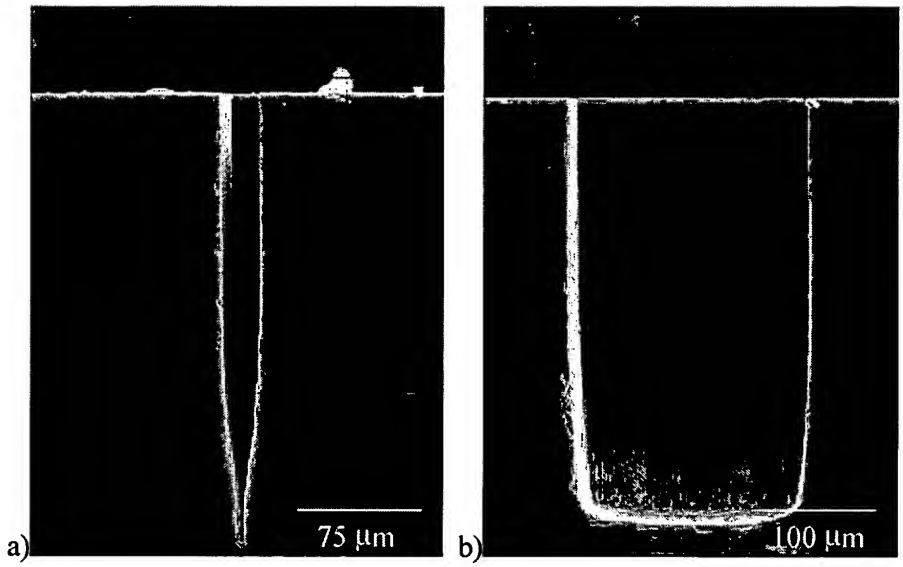


Figure 2-9. Etch profile for rectangles of dimensions 200 µm × L, with a) L = 20 µm and b) L = 2000 µm. The etch used was SMOODEEP for 80 min at 5% exposure density.

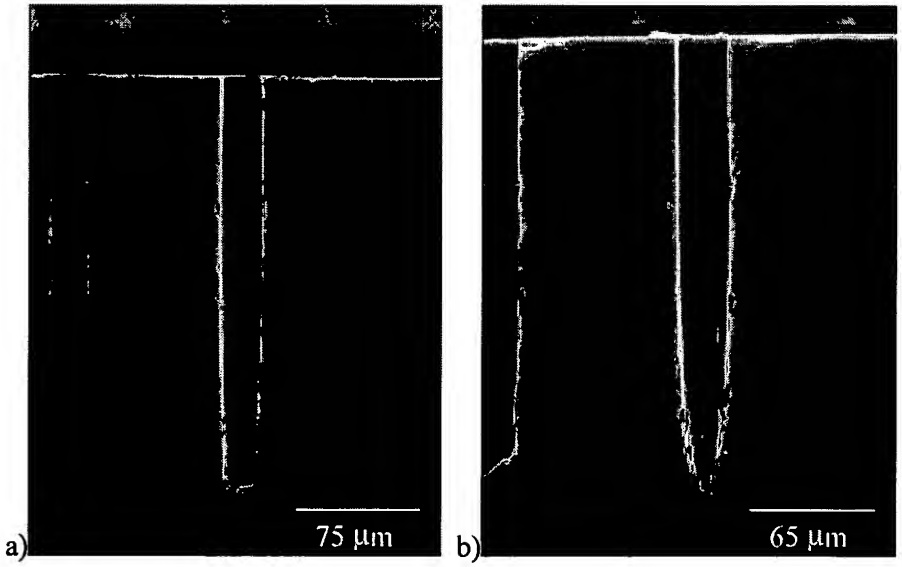


Figure 2-10. Twenty micron squares etched for 80 min with recipe a) DEEP (12 W bottom power) and b) SMOODEEP (8 W bottom power).

The TMPE etch occasionally exhibited micromasking, resulting in very rough bases (Figure 2-11). This occurs when small spots within the region to be etched are masked while the rest of the silicon in the pattern is etched. This was not consistently observed for a given wafer, hole size or etch recipe. Causes have been attributed to incomplete developing of the resist mask, native oxide, or operating conditions which lead to very narrow ion angular distributions [62, 64].

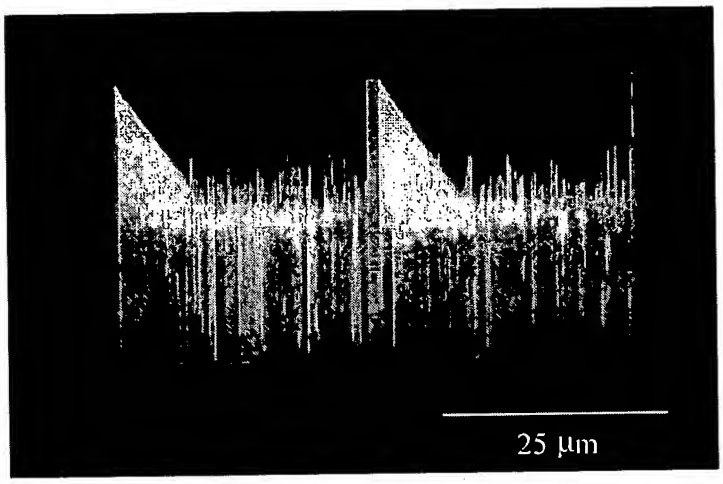


Figure 2-11. Black grass caused by micromasking. SMOOSHALL was run for 30 minutes but a hydrofluoric acid etch to remove native oxide was not performed. Image courtesy of Aaron Partridge.

2.3.3. Side Wall Etching

For aggressive etches of large areas an increased probability of localized side wall etching is observed. Fluorine spontaneously etches so it is able to etch laterally, without direct ion bombardment to activate its reaction with silicon. This was only observed on large areas (one side greater than 200 µm) and for 80 minute etches with DEEP. Figure 2-12 demonstrates a worst case example. This is possibly due to the balance between passivation and etching being altered under certain geometrical conditions such as large area etching. DEEP is the most aggressive etch with the longest etch time per cycle, so it is more likely to see sidewall passivation failure. Researchers have reported that using an oxide mask, with or without a photoresist mask on top, can reduce this effect [62].

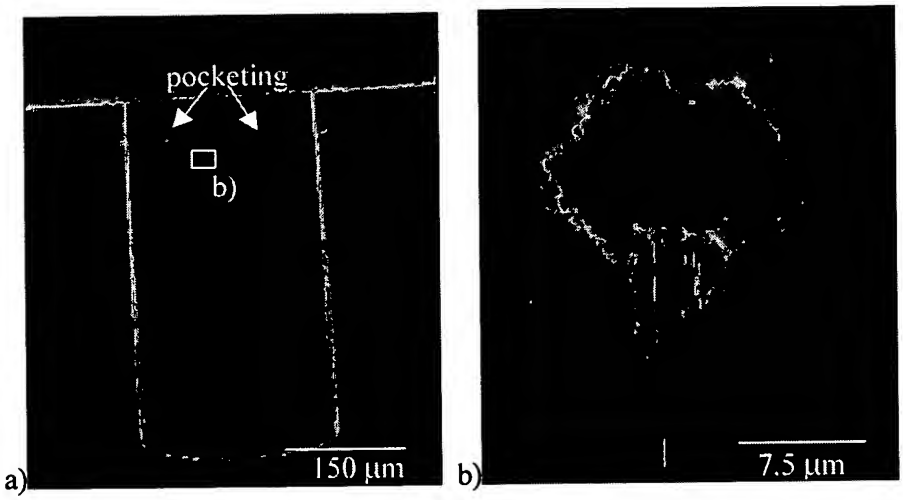


Figure 2-12. a) Etch profiles showing pocketing caused by entrance mask failure using 80 min of recipe DEEP and b) a close up of a sidewall passivation failure.

The high selectivity of the etch to oxide (~150:1) makes oxide an effective etch stop. This allows for precise definition of the silicon device layer thickness when a silicon-on-insulator (SOI) wafer is used. When etching mask patterns with different sized regions, ARDE effects create different etch rates and thus over-etching of larger areas (see Section 2.3.1). However, over-etching at the oxide interface results in aggressive side wall etching (Figure 2-13). This oxide charges and deflects ions laterally, which occurs for both narrow and large etched openings. This charging of a dielectric etch stop is common to many plasma etches, but is accentuated by the high plasma densities used in TMICP etching [65, 66]. This issue will be further addressed in the next chapter.

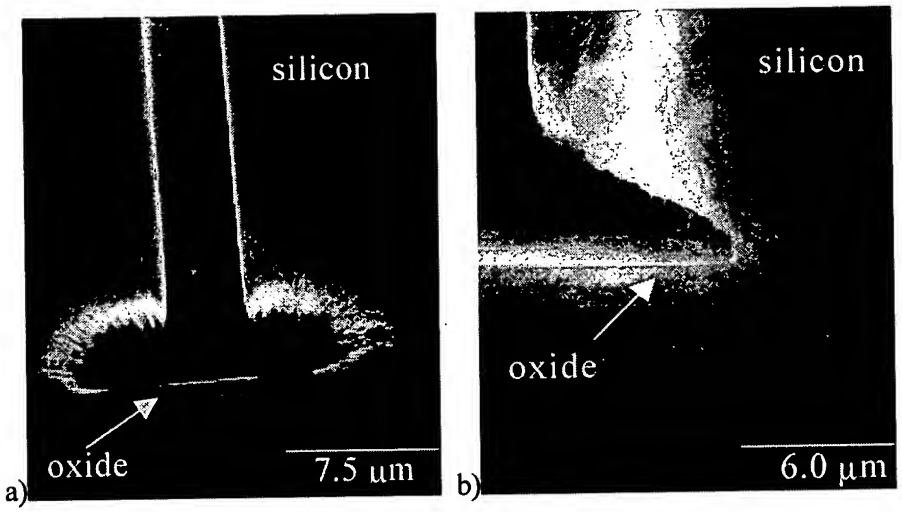


Figure 2-13. Lateral silicon etching at an oxide stop due to overetching in a) a narrow trench and b) a wide trench. Images courtesy of Aaron Partridge.

2.4. Design Implications

These characterization results have important implications for the design of silicon sensors using TMICP deep etching. Silicon etches hundreds of microns deep are obtainable with reasonably thick soft masks (8 μm). The requirements for a TMICP silicon etch depend greatly on the application, as some may need precise profile control with a high aspect ratio and high etch rate, while others may need smooth side walls and a clean oxide stop. However, a general requirement for deep etching applications is knowledge of the silicon etch rate for a particular mask design.

Etch "lag curves" have great design utility, particularly for deep etches (greater than 100 μm) where ARDE effects are most pronounced. To etch uniform depths, it is best to use the same size of exposed regions in sparse densities. Large variations in the size of the exposed regions to be etched can lead to large variations in depth and severe lateral etching when stopping on a dielectric. For larger patterns (greater than 100 μm) and shallower etch depths, lag is less pronounced, and patterns with different size exposed regions should etch at a uniform rate.

Accurate knowledge of these lag curves can be used to design for different depths for applications such as final die separation. A very cumbersome and often low-yield final processing step in released structure fabrication is separating the individual chip die

from the original processed wafer. The standard method is to use a wafer dicing saw, which involves vacuum handling, and cooling jets of water for the blade. Protecting released structures, especially membranes, in this environment is difficult, often involving application of adhesive layers which are difficult to remove, essentially reproducing the basic release problem. With knowledge of the lag curve, a single deep etch can be used to etch a trench for a device and simultaneously etch through-hole lanes around the die. A simple tab can be left so that each die can be manually snapped free, with high yield. Details on how to use through-wafer silicon etches for releasing structures will be covered in the next chapter.

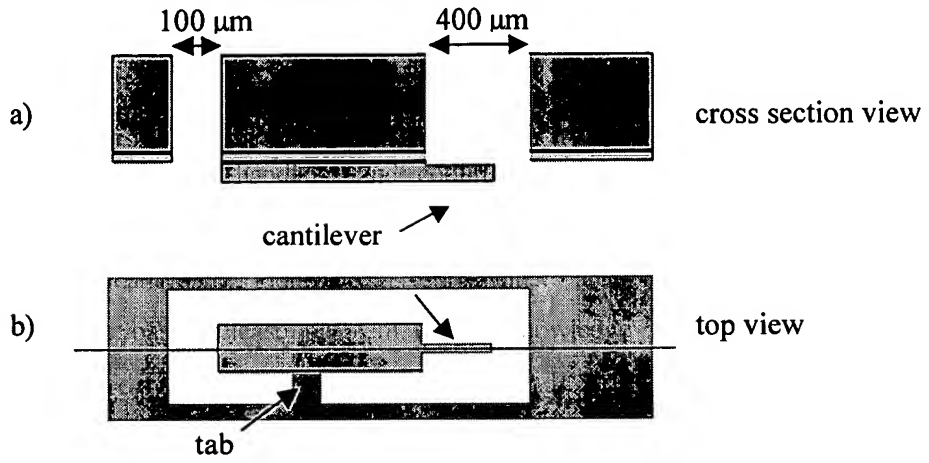


Figure 2-14. Lag curve information is used to design trenches which surround the chip. a) Cross section and b) top view.

2.5. Conclusion

Measurements summarizing the deep etching characteristics of a TMICP process were presented. Silicon etch rate dependencies on pattern size, density, and time were characterized for aiding in the design of masks for device fabrication. Deep silicon etches hundreds of microns deep and aspect ratios of up to 20:1 were demonstrated with this system. Outstanding issues such as profile control and side wall etching were introduced.

While detailed modeling of the TMICP process has not been reported, other groups are pursuing experimental characterization experiments. The most comprehensive is by Ayon et al., as many process parameters were varied to measure etch rate and

profile dependencies [62]. A very important finding was the development of a recipe with reduced lag. This was achieved by slowing down the silicon etch rate and increasing the SF_6 flow rate. This study and others however, were confined to relatively short etch times of less than 15 minutes. Our work here demonstrates that lag is a more severe issue when longer etch times are attempted. Figure 2-6, for example demonstrates 200 μm depth variations on the same wafer.

There is much work being done to improve the TMICP process, as it is becoming a basic tool for silicon sensor fabrication. While researchers work to design new etch recipes for their particular applications, hardware advancements are facilitating many new capabilities. New processes which generate box-like profiles with high silicon etch rates but still maintain high mask selectivity are being aided by new hardware features such as parameter ramping. The SF_6 flow, for example, can be gradually increased as the etch progresses, helping to maintain a box shape [67]. The maximum power of the top electrode is being increased to increase etch rates by more than a factor of two [68, 69]. Recipes with improved side wall passivation are being developed, but lateral etching at a dielectric etch stop is still a troublesome issue. Recently industry has introduced a hardware approach to this problem by applying a low frequency modulation to the bottom power to reduce charging effects [70]. The next chapter presents an alternative solution that uses standard hardware.

Chapter 3: Cantilever Release

In this chapter, the TMICP etching described in the previous chapter is extended to through-wafer depths. We focus on the general problem of releasing microfabricated structures, demonstrating a novel anisotropic, dry release of a microfabricated cantilever from the backside of the wafer. Techniques to overcome key challenges in etch stop control, uniformity and wafer handling were developed to accurately release two-dimensional arrays of cantilevers with high yield and uniformity.

3.1. Motivation

The importance of released sensors such as membranes and cantilevers was introduced in Chapter 1. Fabricating these devices requires a "release" from the substrate, by removing material beneath the sensors, so that they are free to deflect up and down or side to side. An important criteria is underside clearance. If a sensor needs to deflect down towards the substrate, sufficient amounts of material need to be removed. If access to the substrate side of the sensor is required, such as for optical displacement detection, then removal of all of the substrate material beneath the sensor is required.

Conventional wet release processes are difficult to mask and difficult to integrate, particularly for devices which are soft or metallized. Back-side releases are restricted to crystal planes and do not allow high-density designs for arrays of released structures. Dry, anisotropic releases address these issues, which are particularly important for device arrays such as scanning probe cantilevers.

3.1.1. Wet Release Challenges

A large class of microfabricated devices have deflecting membranes or legs for sensing or actuation. Because semiconductor-based, thin film subtractive processes are used, fabrication of this free-standing structure generally requires a release step. If clearances on the order of a few microns or less are adequate, sacrificial thin film techniques are often used. A sacrificial layer beneath the device, such as silicon dioxide is etched in a highly selective wet etchant such as hydrofluoric acid. Stiction, especially for long and thin structures, often plagues this technique, due to surface tension associated with a wet release. The wet ambient also places very strict materials constraints, as metals corrode in many dielectric etchants. Following the wet release with a critical point dry etch avoids many stiction issues, but requires specialized equipment.

A backside release is appropriate when access to the sensor underside is needed. The deflection of a cantilever, introduced in Chapter 1, can be monitored with a laser deflection from the backside. As described in Section 2.1.1, wet etching with TMAH or KOH can be used to etch through an entire silicon wafer. This chemically driven etch is very selective and cleanly stops at silicon dioxide underneath the structure to be released. However, protecting the wafer, particularly the device side opposite the etch side, is very challenging during the prolonged (multiple hours) through-wafer etch. Protective organic films such as photoresist or polyimide are most convenient to deposit and simplest to integrate into a process, but tend to delaminate and fail during long wet etches, reducing yields. High-temperature deposited thin films like silicon oxide and nitride can be used as masks [71] but with corresponding tradeoffs in metallization flexibility, as most metals cannot survive normal chemical vapor deposition (CVD) processing temperatures (500 – 800°C). Refractory metals such as tungsten can withstand upward of 1000°C temperatures, but adhesion issues, lower resistance and reduced availability are hindrants.

3.1.2. Advantages of an Anisotropic Release

Backside wet releases are restricted to crystallographic planes, as they leave holes at 55° angles to the surface. The mask on the backside must be larger than the release side, increasing the required separation between neighboring release areas. This reduces the potential device packing density, which is a key criterion in arrays. Release regions

which have curves in the substrate plane, important for released membrane designs and for controlling stress gradients, are not readily achieved with wet etched releases, again because of variable etch rates between silicon crystal planes. An anisotropic silicon etch, etching 90° to the surface, allows for one-to-one pattern transfer between a backside resist and the resulting release region, permitting increased packing densities and curved shapes.

The sensitivity and versatility of cantilevers, and the potential applications for cantilever arrays were both introduced in Section 1.1. Specific requirements for an array vary with application, but generally include the fabrication of cantilevers with high yield and density, and a method of addressing each cantilever electrically for sensing and/or actuation. To release cantilevers in a 100 μm × 500 μm region on a 500 μm thick wafer, an anisotropic release enables hundred fold improvement in tip densities over wet releases [72], as suggested by Figure 3-1 and Figure 3-2.

A two-dimensional array of cantilevers with through-wafer interconnects would permit wire-bonding from the backside of the chip, away from the tips (see Figure 1-2). Full fabrication of such a device is described in the next chapter.

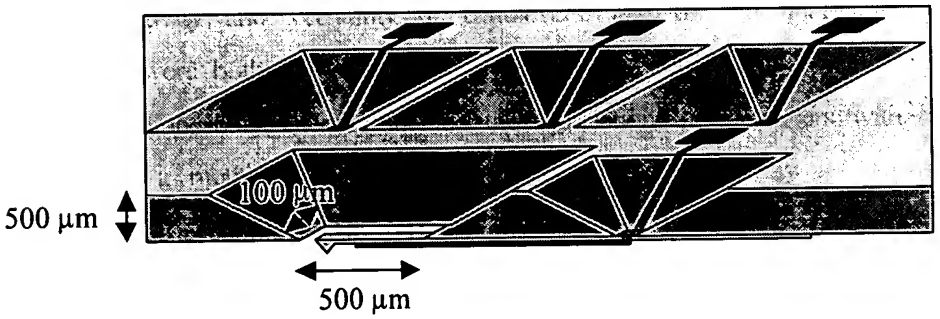


Figure 3-1. Drawing of a wet released cantilever and its through-wafer electrical contacts (with four leads.) For a 100 μm × 500 μm release region with one cantilever per release region on a 500 μm thick wafer, tip densities are limited to less than 0.3 tips/mm^2.

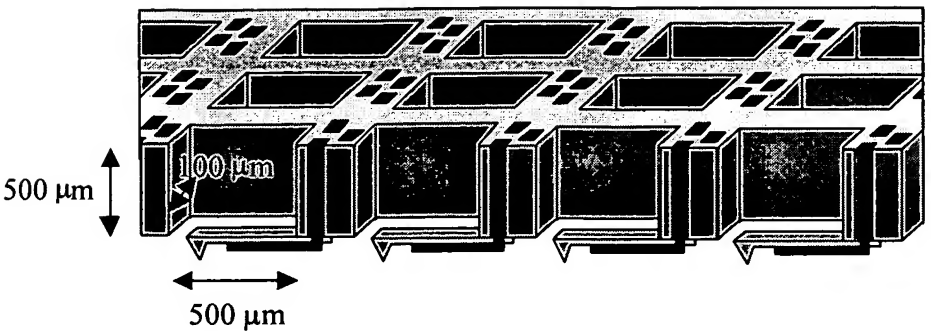


Figure 3-2. Cross section drawing of anisotropic released cantilevers with through-wafer electrical contacts. For a 100 μm × 500 μm release region with one cantilever per release region on a 500 μm thick wafer, tip densities of greater than 20 tips/mm^2 are achievable.

3.2. Release Process

The cantilever dry release process, summarized in Figure 3-3, starts with a 4 in silicon-on-insulator (SOI) wafer or a layer of polysilicon on silicon dioxide. First the front-side device to be released is fabricated. This could include integrated sensors, actuators, and on-chip CMOS circuitry. To demonstrate the release process, simple optical detection cantilevers (200-400 μm long, 5-50 μm wide and 1-3 μm thick) without integrated sensors were fabricated. These are soft structures that require delicate handling to avoid damaging and a precise release to accurately define mechanical properties. A process that can successfully release these cantilevers is useful for similar devices, as well as for larger, thicker devices.

The cantilevers are then coated with a sacrificial support layer, such as photoresist or polyimide, for the final release. The backside of the wafer, polished or unpolished, is patterned with a backside release mask of 8 μm photoresist (Shipley AZ4620). A·TMICP etcher, using recipe DEEP described in Table 2-1, is used to make an anisotropic etch through the wafer, stopping on the buried oxide. The buried oxide layer is then etched in a concentrated hydrofluoric acid (HF) vapor, performed at room temperature and pressure. With minimal surface tension effects, the vapor reaches the bottom of the high aspect ratio holes more easily than wet etchants. Brief heating of the wafer prior to etching reduces water condensation on the wafer, making more sophisticated HF vapor etching techniques unnecessary [73]. The photoresist and polyimide layers above the cantilevers provide sufficient support for a water rinse. Finally the top layer photoresist

is stripped in oxygen plasma to free the cantilevers, enabling a high-yield dry release (Figure 3-4).

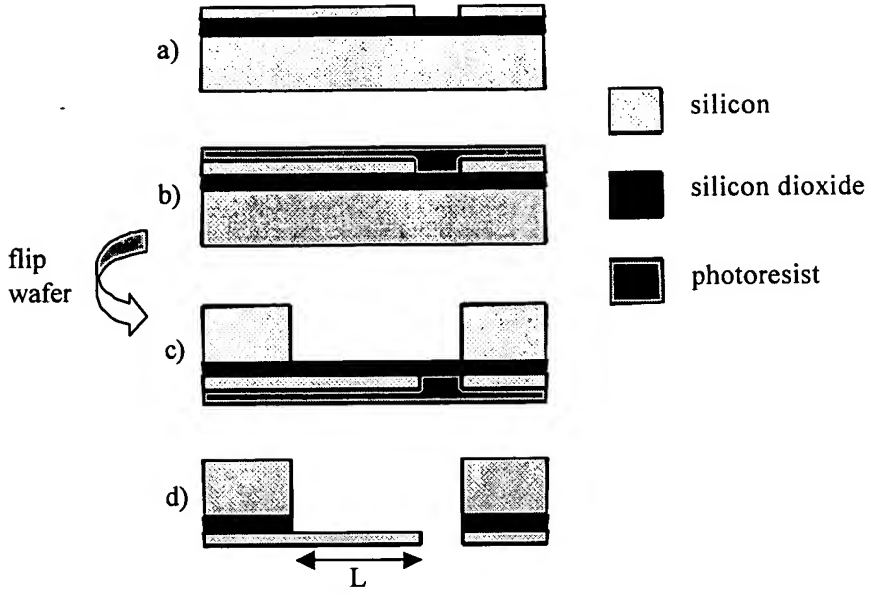


Figure 3-3. Cantilever release process. a) Pattern cantilevers into device layer. b) Coat with support resist. c) Pattern backside and TMICP etch through wafer stopping on buried oxide layer. d) HF vapor etch the oxide and plasma etch the resist for final release.

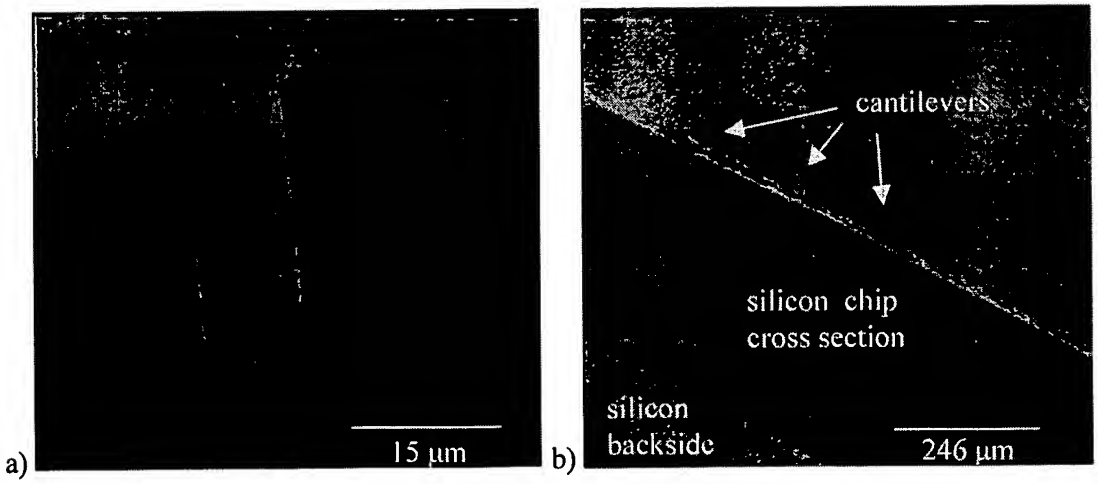


Figure 3-4. SEM image of released cantilevers from a) the top and b) the underside.

3.3. Backside Etch Stop Control

The accuracy of the through-wafer etch determines the accuracy of the device release, which determines the effective length of the device ("L" in Figure 3-3d). For released devices this determines important mechanical properties such as the mechanical resonance, spring constant, and region of maximum stress. The piezoresistors are placed where the stress is concentrated. Being able to accurately release structures is thus critical for realizing device designs. When device arrays are fabricated, consistency as well as accuracy are needed across both a die and a wafer.

Initial release attempts with this process were accurate to less than 5 μm and varied by more than 20 μm across the wafer. This local control for one device, achieved with careful etch timing, may be adequate for some single device designs, but for cantilever arrays it leads to variable resonance, sensitivity, and quality factors (due to clamping losses). Later, in Section 4.3.1, equations describing the mechanical properties of cantilevers are presented, and the strong dependence on cantilever length will be evident. The backside lithography alignment is performed with a contact mask in our lab and is in practice accurate to ± 2 μm. When etching through 500 μm thick wafers, an anisotropy error of 0.3° leads to 3 μm lateral displacement at the release side. While this explains the accuracy, the consistency of greater than 20 μm is due to lateral silicon etching at the oxide interface, which was previously introduced in Section 2.3.3. The silicon etch can be timed to stop at the cantilever base, but over-etching is required to overcome non-uniform silicon etch rates and release devices in other regions of the wafer. Figure 3-4b shows lateral etching of greater than 20 μm under the cantilevers.

Gross misalignment within a die occurs when cantilevers are near a corner of the release region, as demonstrated by Figure 3-5. Similar to loading effects that cause etch lag between different sized etch holes, silicon in the corners tends to etch slower. Thus one way to increase uniformity of a release is to place all devices equidistant from corners. In a cantilever array this corresponds to one hole per cantilever. Figure 3-6 shows a cross section of the two-dimensional cantilever array release pattern, which used this approach.

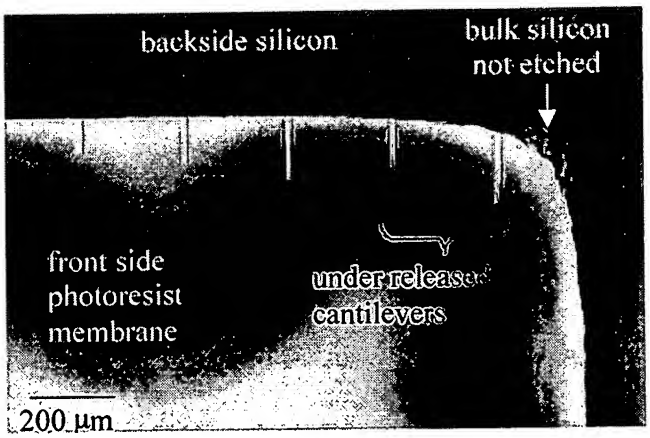


Figure 3-5. Backside view, looking through the wafer to released cantilevers on the frontside. Cantilevers in the corners are under released because of local etch lag effects within the release pattern.

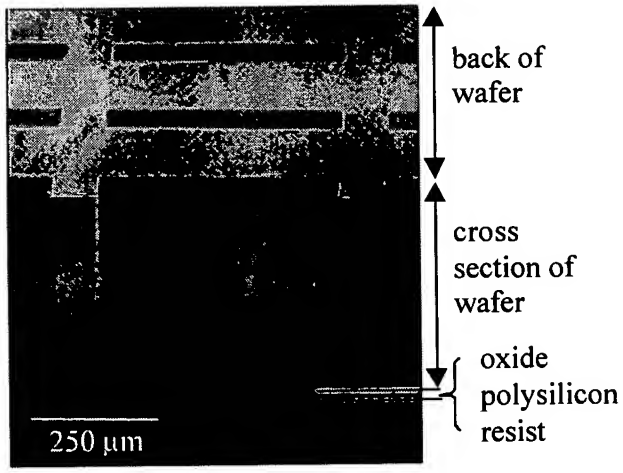


Figure 3-6. Cross section of a single cantilever release region after a TMICP etch through the backside of the wafer. The etch proceeded downward in the picture until reaching the oxide and device layer. The oxide and device layers are supported by thick photoresist.

3.3.1. HBr-Based Etch Stop

When the TMICP etch reaches an oxide or resist etch stop, it starts to etch laterally. The TMICP process is based on fluorine radicals etching silicon. Fluorine has the ability to etch silicon spontaneously, without ion bombardment [74], which is why sidewall passivation is critical for anisotropic etching with SF_6. When the etch reaches

the oxide there is a sudden increase in fluorine radicals as the vertical silicon etching has stopped. This increased fluorine etches through the sidewall passivation at the base of the hole, and etches into the silicon. Charging of the oxide dielectric, which leads to ion deflection, is also thought to contribute to the lateral etching (see Section 2.3.3). Thus the aggressive SF_6/C_4F_8 works well for etching anisotropically and quickly, but does not consistently define the cantilever base throughout the wafer. Figure 3-7 and Figure 3-8 demonstrate how accurate timing for devices in the middle of the wafer severely over-etches devices on the edge of the wafer.

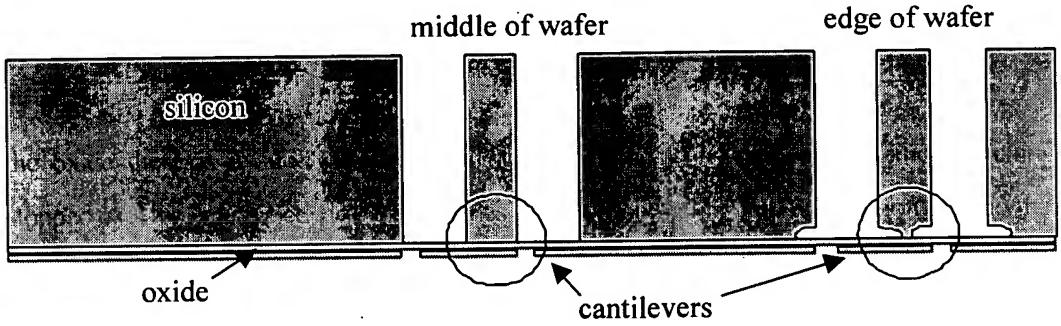


Figure 3-7. Wafer cross-section chematic of etching through a silicon substrate and stopping on an oxide, with nonuniformities in the etch resulting in lateral etching on the edges. SEM images of the circled regions are given in the next figure.

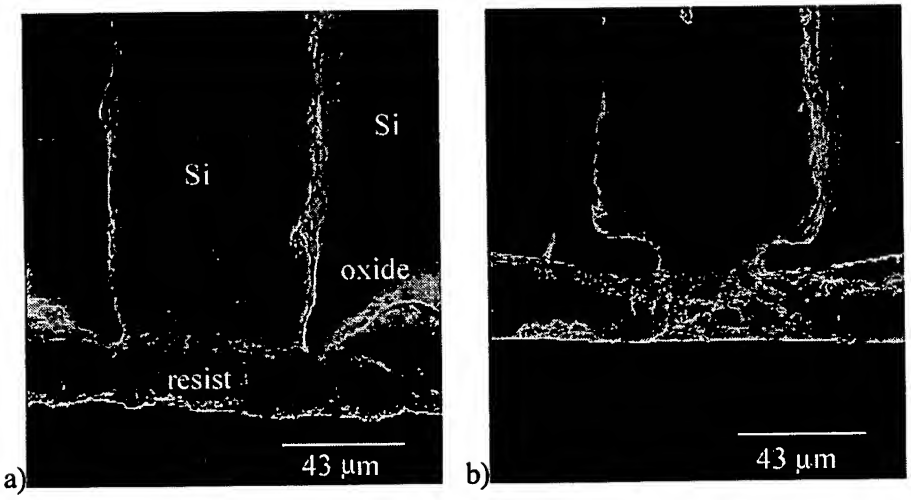


Figure 3-8. a) The aggressive SF_6/C_4F_8 based HDLP etch can be carefully timed for a well defined stop in the middle of the wafer, but b) the edge of the wafer still experiences severe lateral silicon etching. These views have the same orientation as Figure 3-7, with the device layer beneath the oxide.

To control the oxide stop, an HBr-based HDLP etch is used to finish the backside etch (Figure 3-9). The chemistry of this etch does not permit rapid lateral silicon etching at the oxide interface, as ion bombardment is necessary for activation of the silicon etch [74]. First the TMICP SF_6 etch is stopped early so that silicon feet, shown in Figure 3-10 and Figure 3-11, are left at the cantilever bases throughout the wafer. Then another commercial HDLP etcher, also with separate coil and platen RF sources, but without the TMICP process, is used [75]. Operating at 10 millitorr, with an RF coil power of 250 watts and platen power of 60 watts, HBr (150 sccm flow) and O_2 (15 sccm flow) are simultaneously used to etch the remnant silicon feet. Combined with a high silicon-to-oxide etch selectivity (greater than 200:1), controllable rates (3000 Å/min for Si), and high anisotropy, this etch is ideal for clearing out the remnant silicon feet in a controlled manner. Since overetching can be tolerated, the cantilever bases can be well defined throughout the wafer (Figure 3-12).

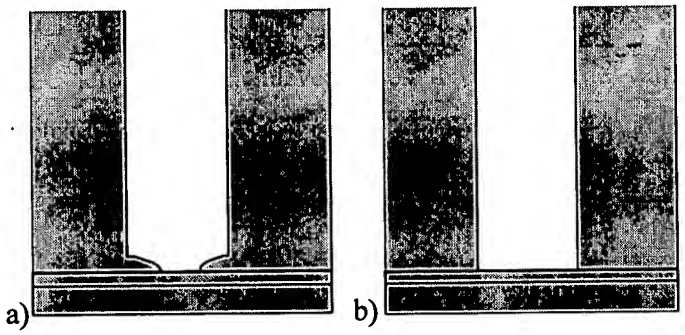


Figure 3-9. Schematic of two-step etch process. a) Etch through wafer with TMICP etch but stop short of completing the release. b) Clean up etch with HBr-based etch.

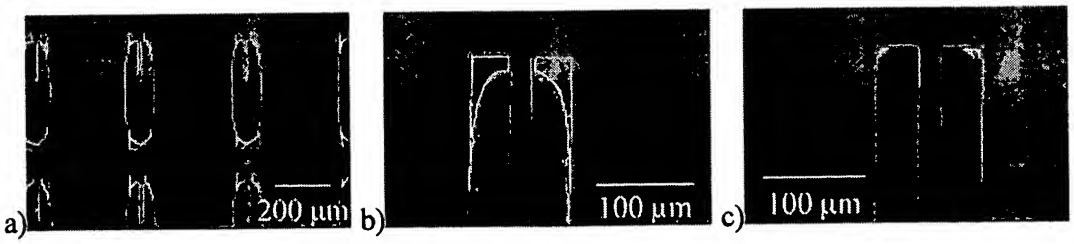


Figure 3-10. Cantilever base viewed from the topside of wafer. a) At low magnification showing part of the array. b) At higher magnification in the middle, and c) at the edge of the wafer.

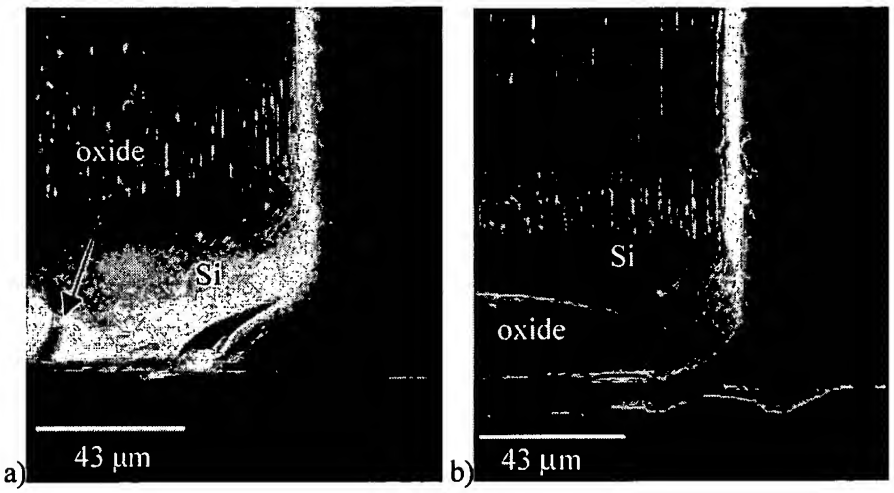


Figure 3-11. The deep etch is timed to leave a silicon foot in a) the center and b) the edge of the wafer. The oxide and device layers are supported by thick photoresist.

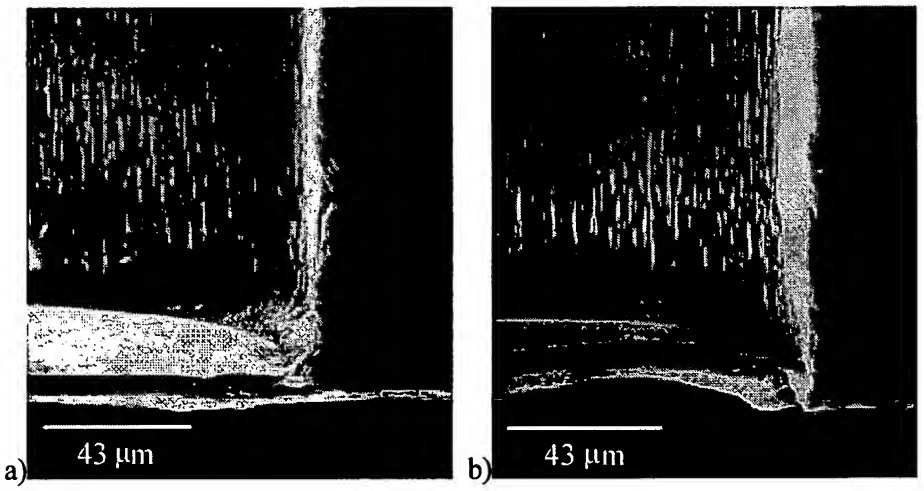


Figure 3-12. The HBr-based HDLP etch clears out the remnant silicon foot in a controlled manner at a) the middle, and b) the edge of the wafer.

A completed cantilever array is shown in Figure 3-13. A density of 5 tips/mm^2 is demonstrated here. The ultimate density depends on the size of the cantilevers and the mechanical integrity of the silicon wafer. For these cantilevers using this release technique, we expect densities of up to 20 tips/mm^2 to be possible. High yields were obtained, as out of 45 die per wafer, typically only 2-3 of the die had single defects. As shown in Figure 3-12, the two-part etch results in a silicon foot length deviation of less

than 5 μm across the entire wafer, which is a significant improvement over the 20 μm variations typical of the SF_6/C_4F_8 etch stop. With longer HBr etching, this variation between the center and edge of the wafer could be reduced, especially since the chemistry of the etch tolerates overetching.

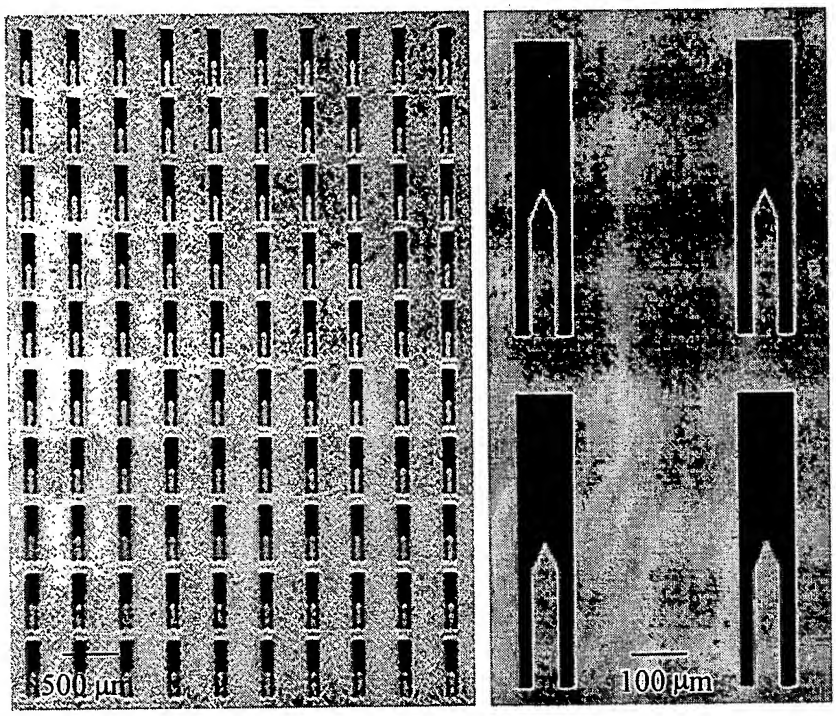


Figure 3-13. a) Optical photographs of a finished 10 × 10 array of cantilevers, with release regions of 100 μm × 500 μm. b) Close up of the same array. The cantilevers are made of polysilicon, and are 50 μm wide, 200 μm long, and 1.6 μm wide.

3.4. Through-Wafer Handling Challenges

Using TMICP etching to form holes tens or even a couple hundreds of microns deep, at most about half the thickness of a 4-in silicon wafer, is in many ways simply an extension of current semiconductor plasma etching techniques. A soft (photoresist) or hard (silicon nitride or silicon oxide) mask is patterned on one side of the wafer, and all etching occurs only from that side. The handling, cooling, clamping, and chamber systems are all designed for such single-sided processing, as it is assumed that the bottom of the wafer is clean silicon and not a device layer. Plasma etching through-holes, such as

for device releasing or through-wafer interconnects, however, requires improvements in wafer handling techniques.

3.4.1. Through-Hole Etching Issuess

There are numerous problems associated with very deep to through-wafer etching. Holes reaching through to the backside of the wafer expose the chuck and possibly the backside gas coolant (usually helium) to the process environment. This can cause damage to the chuck and contaminate the process chamber. In the trench the helium displaces the process gases and dramatically alters the etch. To prevent this, thin film layers which stop the etch and protect the chuck are placed on the bottom side of the process wafer. Thus, to protect the chuck and process chamber, the etch needs to be carefully monitored such that it does not punch through this stop layer. The thickness and fabrication requirements for this thin film can place severe design restrictions on process wafers.

Very deep to through-wafer holes also make it more difficult to unload process wafers. Typically pins rise out of the chuck beneath the wafer, to lift the wafer up so that a spatula can reach underneath the process wafer to take it out of the process chamber. During this motion the mechanical integrity of the wafer needs to be such that the pins can smoothly lift the wafer. This can severely limit design of the holes and places surface requirements on the back surface of the process wafer. For example, holes need to be out of the path of the pins and large holes are dangerous because of weak structural integrity. Similarly, the backside surface of the wafer needs to be such that the process wafer will not stick to the chuck and interfere with the pin lifting action of the unloading procedure. This places serious design requirements on the permissible materials used on the backside of the wafer. For example, photoresist and polyimide cannot be used on the backside of the wafer because they can easily overheat and stick to the chuck.

3.4.2. Support Wafer

A common solution to the above problems is the backing wafer. A backing wafer is another silicon wafer that is adhered beneath the original process wafer. Photoresist is commonly used to adhere the two wafers. This wafer is typically used only for the very deep/through wafer etch, and is removed after completion of the etch. The physical bulk

of the backing wafer protects the chuck in case of possible puncture through the stop layer. Also, because the backing wafer is not part of the original process wafer device, it is not a design restriction to keep its underside smooth and clean. As described above, a sticky or bumpy process wafer underside could have problems loading or unloading.

Unfortunately, this backing wafer solution is precarious and severely restricts process flexibility. When photoresist is used to adhere the process wafer to the backing wafer, physical pressure needs to be applied between the two wafers to aid adhesion. This is a very unusual semiconductor wafer processing step which involves physically touching the top surface of the process wafer. Contamination and disruption of the thin film patterns on the top of the process wafer are critical concerns with this adhesion process. Once the wafers are attached, they are often baked to harden the adhesion layer of resist. This extra heating step complicates processing for the masking thin films on the processing wafer, and can lead to cracking. Once the wafer is ready to be inserted in the semiconductor processing equipment, other problems can arise. Delamination of the process wafer from the support wafer can occur because of heating during the long etch or from poor initial adhesion. Such problems are often catastrophic, leading to broken process wafers and costly equipment maintenance. Removal of the backing wafer involves prolonged acetone bathing, which results in a wet release and its associated problems (see Section 3.1.1).

3.4.3. Reusable Wafer Support

To eliminate many of the above problems, a reusable, non-adhesive wafer support was designed [76]. A disk for the wafer to rest on, with an opening for underside helium gas and an o-ring for sealing, can be used as a wafer support (Figure 3-14). A ring on top of the wafer, held in place by pins, protects the edge of the wafer from being etched. Preventing mask failures on the edge of the wafer is particularly important because this is where cracks start. Such a holder is compatible with both mechanical and electrostatic chucks common to plasma etchers. An aluminum version was constructed for use in these experiments. Ceramic is less prone to metallic sputtering in the chamber and is thus a preferred material, but requires specialized machining.

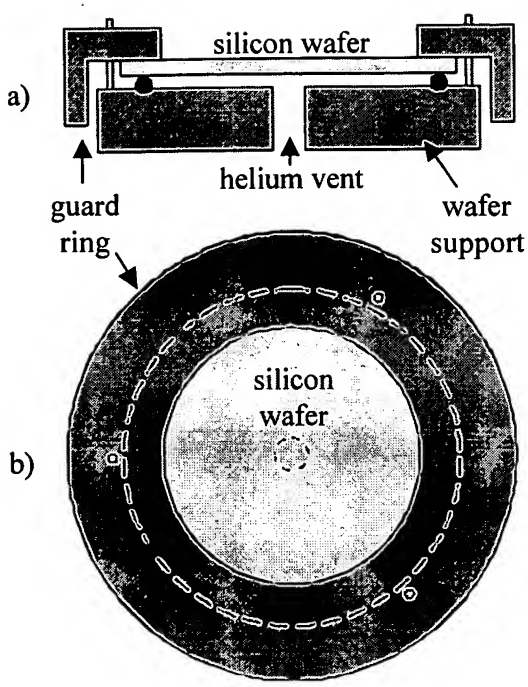


Figure 3-14. Schematic of through-wafer etching holder. a) Cross-section and b) top-view.

The support wafer permits increased flexibility of the backside surface material of the process wafer, particularly for through-wafer release processes. For example, rough and potentially adhesive backside layers such as photoresist and polyimide are now permissible without the loading, clamping, and unloading problems associated with backing wafers.

The support wafer permits increased flexibility in the physical design and construction of process wafers for very deep etching. The physical integrity of the wafer is less of a concern because the support wafer protects the equipment chamber and its chuck from damage due to stray wafer chips (pieces of a process wafer which may be freed during processing). The possibility of leaving residue on the wafer chuck is greatly decreased, reducing maintenance and the chances of declamping for the next process wafer.

3.5. Conclusion

The release process presented here demonstrates the advantages of a dry, anisotropic release. Improved release accuracy can be achieved by using small release

regions for single devices, and by combining an aggressive TMICP silicon etch with an HBr etch. The process is low-temperature compatible and uses simple photoresist masks. Recently industry has developed another etch recipe which alters the plasma frequency for use as a second etch with minimal lateral etching [70]. An experimental comparison of these two approaches is worth investigating.

A disadvantage of a through-wafer etch release is the significantly long etch times. Researchers are pushing silicon plasma etch rates (up to two times higher) through hardware improvements [68]. However, the process remains expensive because one wafer is processed at a time. Wet etches are economical because many wafers can be processed in parallel, but they have the challenges described in Section 3.1.1. In general, the through-wafer approach also has wafer integrity issues, especially for high-density patterns and die-packing, as significant portions of the wafer are removed. If backside access is not required and oxide encapsulation is compatible, then a front-side release using TMAH or XeF_2 may be more appropriate, as the majority of the silicon wafer will remain intact [5, 41].

Chapter 4: Sensor Arrays

High-density electrical through-wafer interconnects (ETWI) are incorporated into a two-dimensional micromachined cantilever array. The ETWI are fabricated using the previously discussed time-multiplexed inductively coupled (TMICP) etch process, passive electrical isolation, and tungsten as a conductor. Each cantilever has piezoresistive deflection sensors and high-aspect ratio silicon tips. The cantilevers are released using techniques described in Chapter 3. This integration of cantilevers, tips, and interconnects enables the operation of a high-density two-dimensional scanning probe array over large areas.

4.1. Purpose - 2D Cantilever Arrays

Scanning probe devices, previously described in Chapter 1, take advantage of high spatial resolution and high force resolution to make significant contributions in a variety of fields. While the sensitivity of these techniques is most impressive, the throughput and sensing area are hindered by their reliance on serial scanning. The ability to fabricate large, densely packed, two-dimensional arrays of sensors would address this problem, as arrays increase signal throughput without sacrificing the spatial sensitivity of the individual sensor. As detailed in Chapter 1, this is true for both scanning and non-scanning applications, covering diverse areas in imaging, lithography, data storage, and biochemistry.

Linear (1D) probe arrays have been previously demonstrated with cantilevers operating nominally at a 15° angle to the sample [18, 77]. This enables close spacing between the tip and sample, while allowing the bond pads to be on the same side of the wafer as the tip (Figure 4-1). However, two-dimensional arrays require parallel planar alignment to the sample. In previous 2D arrays, bond pads with the associated wiring were on the same side of the wafer as the tips [78]. This hinders scanning flexibility when the sample region is larger than the cantilever array die. In addition, for operation in liquids and gases, protecting the wire bonds is a cumbersome challenge (see Figure 4-2). Recently, ETWI in glass have been integrated with a 2D cantilever array for data storage applications [20]. ETWI serve to move electrical wiring to the backside of the chip and away from the sensor. This is especially important for devices that require high-packing density to maximize throughput. In this thesis, electrical through-wafer interconnects (ETWI) in silicon connect the deflection sensing piezoresistors on the tip side of the wafer with the bond pads on the backside, enabling versatile scanning of arbitrarily sized samples and efficient packaging (Figure 4-2).

The traditional method for observing scanning probe deflection uses a precisely aligned laser beam reflection aimed at the cantilever and then into a photodetector. Such an implementation does not easily scale when many independent cantilevers need to be sensed, as such dense optical systems are complicated to build and align, particularly for 2D arrays [79]. In contrast, piezoresistive sensors change resistance under a stress load, so the geometric challenge of optical detection is replaced by the challenge of making electrical circuits to measure resistance changes. Multiplexing electronically has already been implemented in piezoresistive device arrays [5]. Piezoresistive deflection sensors tend be less sensitive than optical detection methods, but optimizing piezoresistive sensitivity is an active area of research [80]. We chose to implement piezoresistive detection for scanning probe arrays because of ease of implementation and scaling.

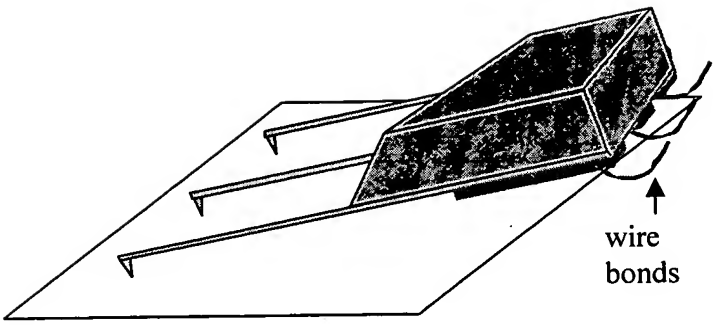


Figure 4-1. A linear cantilever array, positioned at an oblique angle to the samples to leave space for tip-side wire bonds.

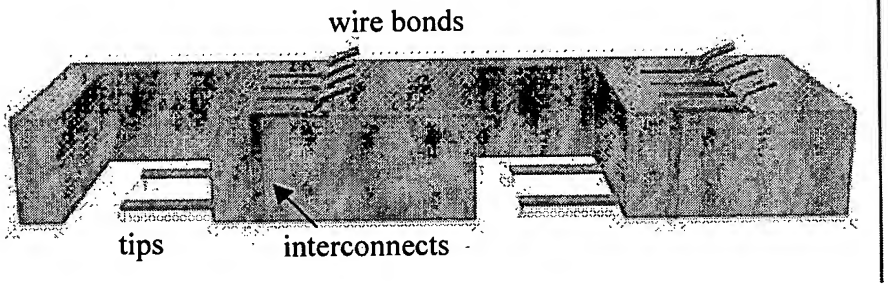


Figure 4-2. A 2D array of cantilevers with through-wafer interconnects, allowing for wire-bonding and simultaneous contact of multiple rows of tips to the sample.

4.2. Fabrication

The fabrication of the cantilever array with ETWI involves the processing of four major elements: 1) high-aspect ratio silicon tips, 2) piezoresistor and contact implants, 3) through-wafer interconnects to the piezoresistive sensors, and 4) anisotropic dry release of cantilevers. The full device process requires eleven lithography steps. For a detailed summary see Appendix B.

4.2.1. High-Aspect Ratio Tips

The starting substrate is a silicon-on-insulator wafer with a 20 μm silicon device layer and 2 μm buried oxide on a 400 μm silicon handle wafer. High-aspect ratio tips are formed in the device layer silicon in a multi-step etch process, combining isotropic and anisotropic etching with one mask. Unlike previous tip fabrication work for linear arrays [50, 81-83], tall tips (greater than 5 μm) with good uniformity are critical for aiding array

2D alignment to the sample. Fabricating uniform tall tips is challenging because process etch rates often vary across the wafer and change with loading.

Tip process development involved attempting to minimize etching time in systems with poor uniformity. Stanford's traditional parallel plate plasma silicon etcher (Drytek) is very non-uniform, with rates varying by more than 10% across a wafer. The multi-step tip process requires precise control of an isotropic etch so that a silicon neck can be carefully thinned, but not too much so that the mask sitting above it falls. Aggressive etches like the TMICP describe in Chapter 2 are too quick to control for this application.

Attempts were made to use TMAH as the isotropic etch, as this was expected to be more uniform than Drytek etching. To control the isotropy such that the neck height is maximized, an anisotropic pillar was first etched with an HBr-based high-density low-pressure (HDLP) etcher (LAM Research) (Figure 4-3). Unfortunately, the TMAH etch rate was too fast and difficult to calibrate for such a short etch (Figure 4-4, Figure 4-5, Figure 4-6). Clean room contamination issues were also a concern, as wafers exposed to such processes were normally not allowed back into mainline machines.

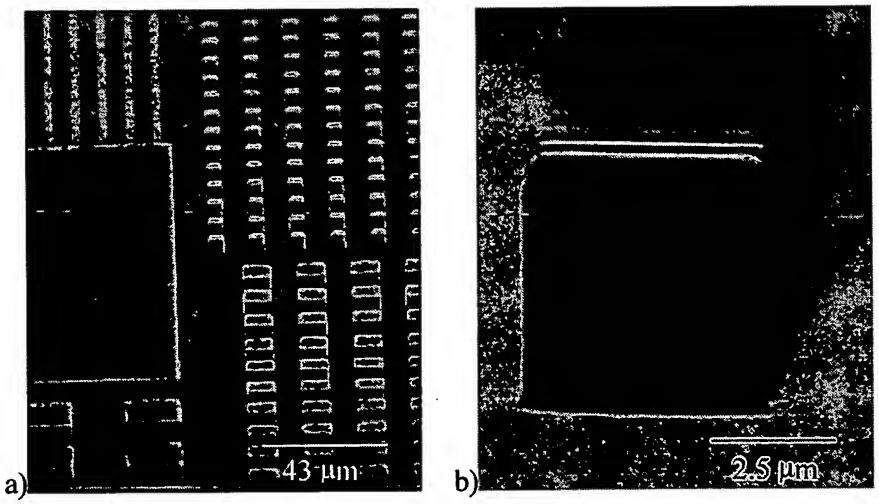


Figure 4-3. Etching a pillar with a vertical plasma etch. a) Tip test mask, with various sizes. b) Close up of a pillar. A one micron oxide mask was used.

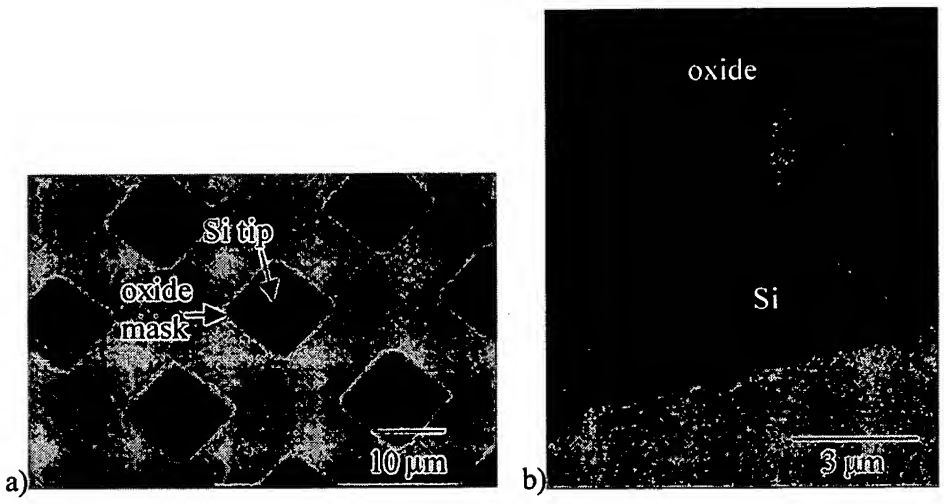


Figure 4-4. After etching the pillar with 10% TMAH for 210 sec. View from a) above the tips, looking through the square oxide mask and b) an SEM cross section.

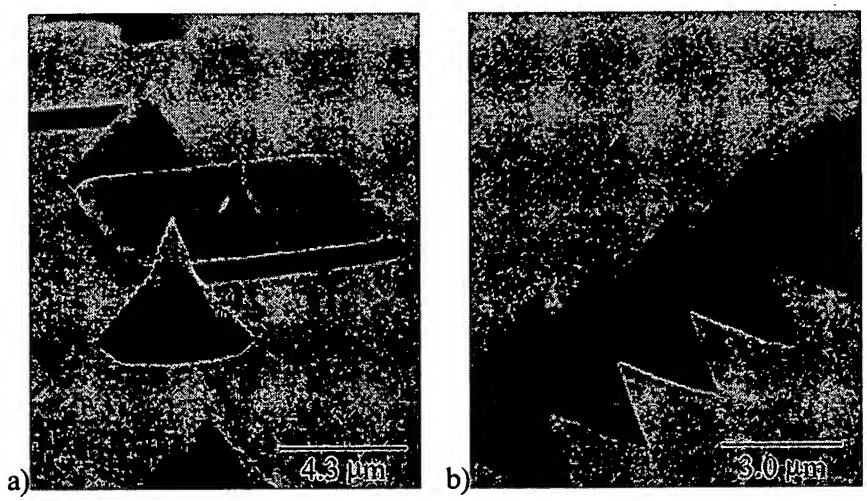


Figure 4-5. After 15 sec more etching beyond Figure 4-4, showing a) a fallen cap and b) 3 - 4 µm tall tips.

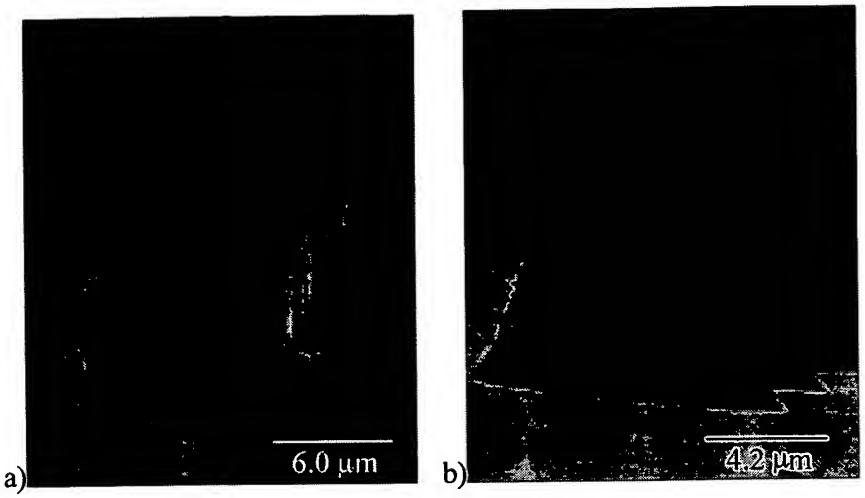


Figure 4-6. Other vertical plasma etch and wet etch combinations. a) LAM plasma etch for 15 min, TMAH for 5 min, LAM plasma etch for 15 min, and then b) 110 sec of TMAH.

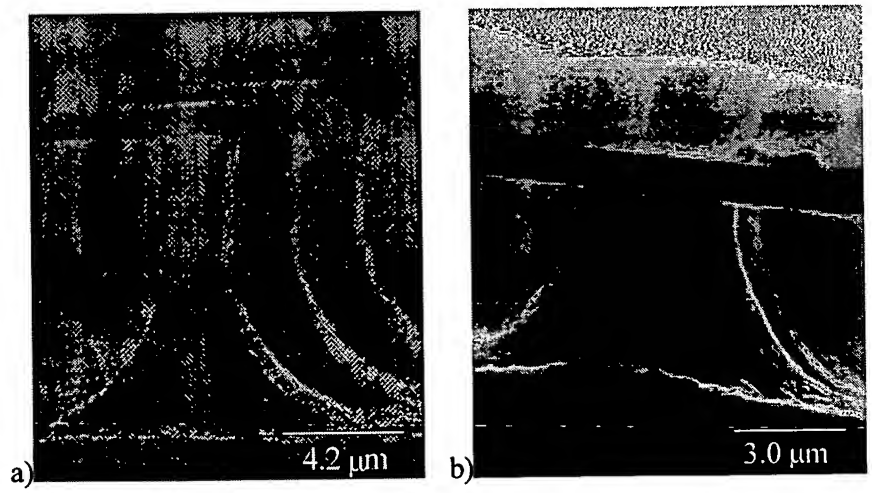


Figure 4-7. Tuning the LAM plasma etch to make a tall tip with SF_6. a) Apex too low, using 15 mtorr pressure and 300 W top power. b) Taller apex, using 50 mtorr pressure and 200 W top power.

The HDLP LAM etcher was known to be very uniform and consistent, as the tool had improved gas, plasma, and temperature uniformity within the etch chamber. The tool was originally designed for anisotropic etching with HBr or Cl. An attempt was made to develop an isotropic SF_6 etch in the LAM etcher. Pressure and ion power were tuned to develop a narrow neck at the top of the pillar, maximizing tip height (Figure 4-7).

Unfortunately, successive anisotropic etches (HBr or Cl) necessary to make the tip taller caused micromasking and rough silicon surfaces (Figure 4-8). It is thought that aluminum in the chamber was reacting with the SF_6 to form nonvolatile compounds. This normally is not an issue in this chamber with HBr and Cl based etches.

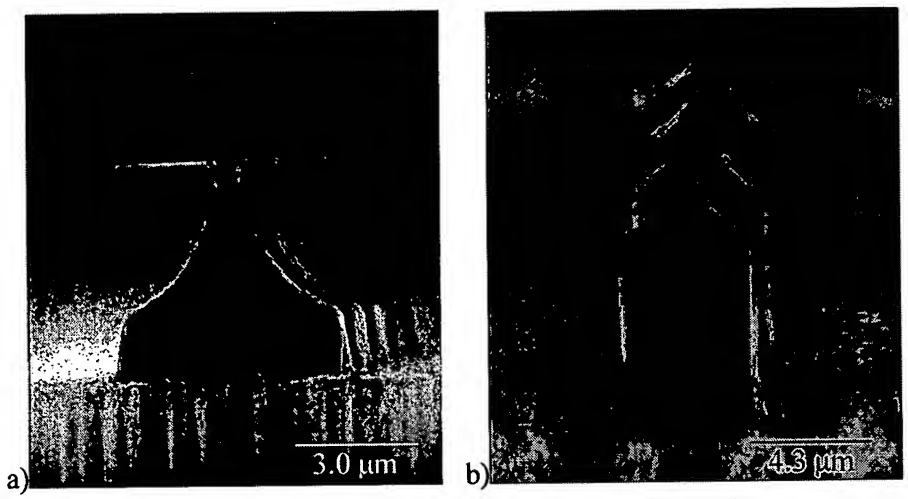


Figure 4-8. An isotropic SF_6 plasma in the LAM etcher followed by an anisotropic HBr etch in the same tool. a) Significant grass formation. b) Removing the grass with an SF_6 plasma in the Drytek works, but still leaves a rough surface.

To address repeatability and surface roughness issues, we returned to the Drytek plasma etcher despite the uniformity issues. The final process used an isotropic plasma etch with SF_6 in the Drytek etcher to narrow the neck under the silicon dioxide mask and then an anisotropic plasma etch (Cl_2/HBr) to control the height of the tip, allowing the flexibility to vary the cantilever thickness. The oxide mask is then removed in buffered hydrofluoric acid (BHF). The tips are sharpened through another isotropic plasma etch with SF_6 in the Drytek, followed by a long oxidation [84]. Another BHF dip is used to strip the oxide. This process was a significant improvement over the previous process because functional tips were fabricated across the wafer, though sharpness varied due to different neck thicknesses.

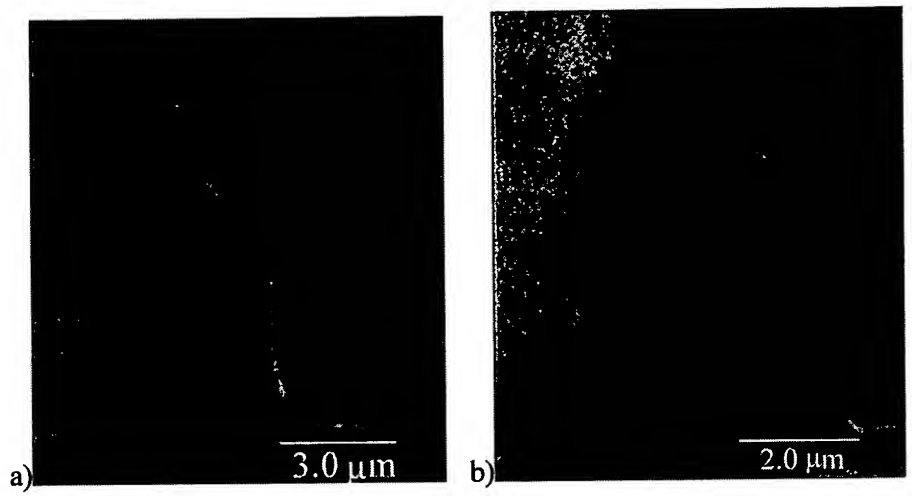


Figure 4-9. Final tip process selected: SF_6 Drytek, HBr LAM, then SF_6 Drytek. Tips are nobby in a) the middle of the wafer, but sharp on b) the edge. The surface is smoother than the SF_6 Lam etches. No micromasking was noticed.

4.2.2. Piezoresistors

To form the piezoresistors, a resist pattern is used to mask boron implants at 40 KeV with a dose of 5×10^{14} cm^{-2}. These parameters place the majority of the dopants near the surface of the cantilever, increasing deflection sensitivity [80]. To insure ohmic contacts to the piezoresistors, a heavy implant at 80 KeV and 5×10^{15} cm^{-2} is performed at the base of the piezoresistors where the contact pads will be located (Figure 4-10a).

4.2.3. Electrical Through-Wafer Interconnects

The via for the electrical through-wafer interconnects (ETWI) is made by anisotropically etching 30 µm square vias through the entire thickness of the wafer using the TMICP etch with recipe DEEP. The first part of this etch is done from the front of the wafer, through the silicon device layer. The buried oxide is then etched in BHF. The majority of the via is etched from the back of the wafer (four hour etch) with another resist mask, which is aligned to the front side using a backside contact aligner (Figure 4-10b). Etching from the frontside first and then the backside serves to simplify buried oxide removal as it is easier to wet the via from the top of the wafer, where the via is most shallow. This also simplifies tip protection, as the tips do not experience a long plasma etch. Hereafter, simple spin-on resist masks were used repeatedly to protect the bottom-side of the wafer, facilitating double-sided wafer processing.

Multiple thin films are then deposited in the via to form the through-wafer interconnect. A half micron of low-pressure chemical vapor deposition (LPCVD) oxide is deposited to serve as a future etch-stop for protecting the silicon tips. Conformal LPCVD silicon nitride (1 μm) is used for via electrical isolation, followed by LPCVD polysilicon (1 μm) for tungsten adhesion. Contacts to the piezoresistors are patterned and CVD tungsten (1 μm) is deposited. Aluminum is sputtered on the backside to aid wire bonding, as tungsten does not adhere well to aluminum or gold bond wires (Figure 4-10c). Unlike previous through-wafer interconnect work which used electrodeposited resist, patterning of the front and back metal is done with conventional spin-on thick photoresist (Shipley AZ4620) [35, 72]. If the resist is spun-on thick (15–20 μm) and baked resist-side down in a convection oven (90°C for one hour), it is able to harden as a membrane over the 30 μm squares. With this resist mask the aluminum is wet etched, and the tungsten, polysilicon, and nitride layers on the tip side and wire bonding side of the wafer are patterned in SF_6 plasma etches (see Figure 4-11). The etch stops on the oxide, preserving the sharp tip, and the oxide is removed in BHF (Figure 4-10d).

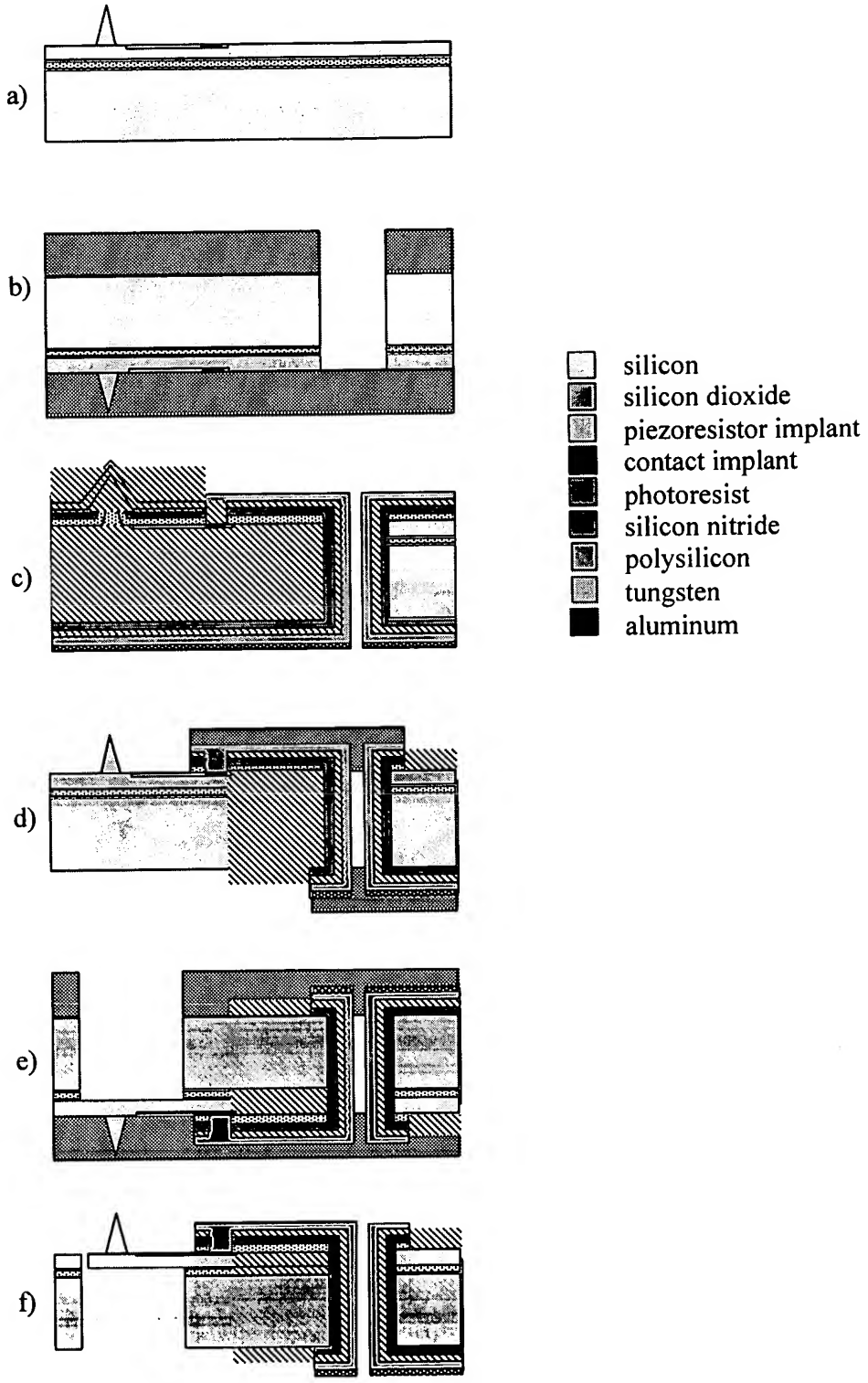


Figure 4-10. Process flow schematic for a 2D array of piezoresistive cantilevers with through-wafer electrical interconnects.

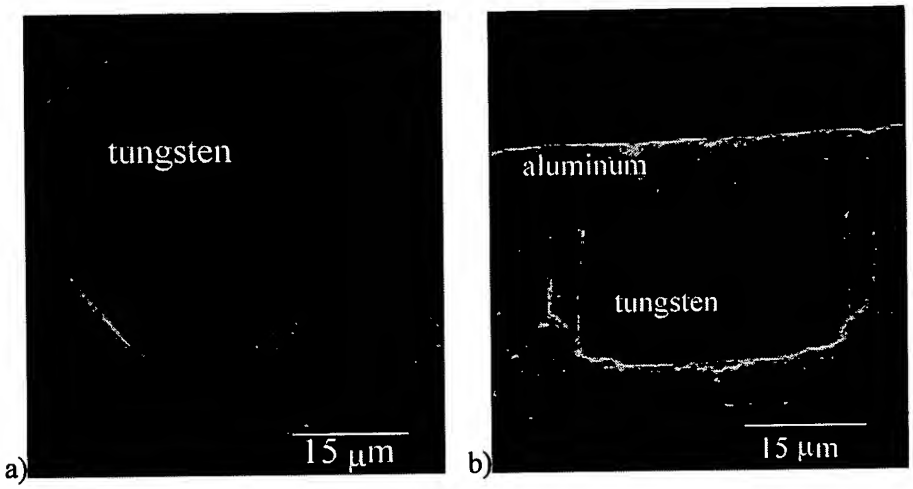


Figure 4-11. Completed interconnects viewed from a) the tips-side and b) the wire-bond side.

4.2.4. Cantilever Release

After completing the ETWI, the cantilevers are released with a backside etch (Figure 4-10e), again using a TMICP etch which stops on the buried oxide. Because resist masks protecting the ETWI were starting to fail during the long TMICP etch through the wafer, the HBr based etch technique used to improve etch uniformity, described in Section 2.3.1, was omitted. The anisotropy of this technique allows for small release regions and thus high cantilever density. The buried oxide is then removed in BHF. The resist that protects the cantilevers is stripped in oxygen plasma for the final release (Figure 4-10f). The cantilevers are far enough from the side of the backside release region to be uniformly released (see Figure 3-5). SEM images of completed cantilever arrays are given in Figure 4-12.

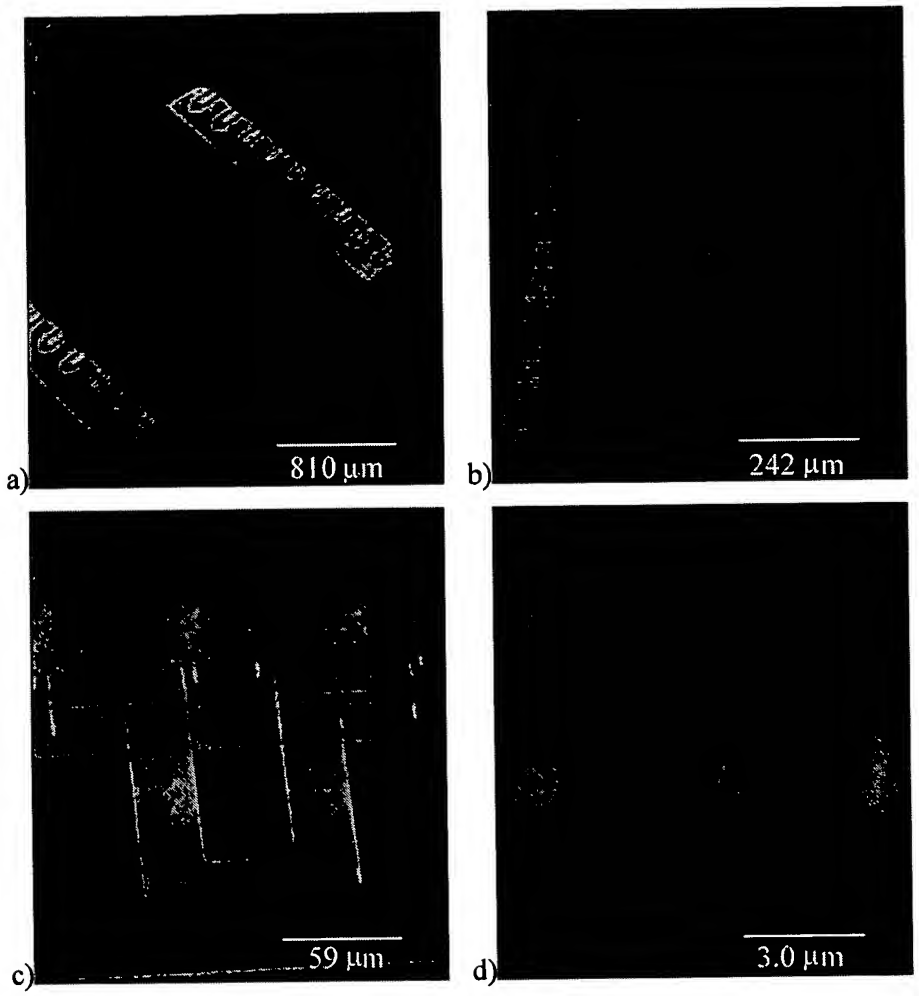


Figure 4-12. A completed array, viewing a) wire-bond side, b) tip-side, c) a single cantilever and d) silicon tip.

4.2.5. Die Release and Packaging

Separating a die from the wafer is often a low-yield step when released devices are involved, as standard wafer-saw techniques require high-pressure water cooling which easily destroys free membranes. Knowledge of the etching rates for different sized trenches allowed design of a die-release trench around each chip. Etching this trench through the wafer, while leaving a 1 mm tab, results in a die which can be cleanly removed with tweezers and a diamond scribe, thus avoiding the wafer saw (see Section 2.4). This die release etch can be combined with the cantilever release etch if the etch rates of the two regions are roughly the same. Severe over-etching to make sure both

regions are completely etched through is not tolerable because the through etch stops on photoresist (see Figure 4-10). All cantilever release regions were greater than 200 μm × 200 μm, placing them in the plateau region of the lag curve (see Figure 2.5), so a 1000 μm wide trench surrounding the die was used as a release trench.

A common package for devices with many interconnects (greater than 20) is a pin grid array (PGA). Open cavity PGA packages surround the chip with bond pads, allowing for many connections with minimal wire-bond length. A cavity down PGA places the chip upside down, facing the pins. For integrated circuit applications this leaves a flat surface for extensive heat sinking. Packaging the 2D chip to enable sample scanning required use of a modified open cavity down PGA package. By drilling a hole through the ceramic package, mounting the chip on the outside, and then wire-bonding through the hole, we were able to have unobstructed access to the plane of silicon tips, as well as mount the chip onto a circuit board (Figure 4-13).

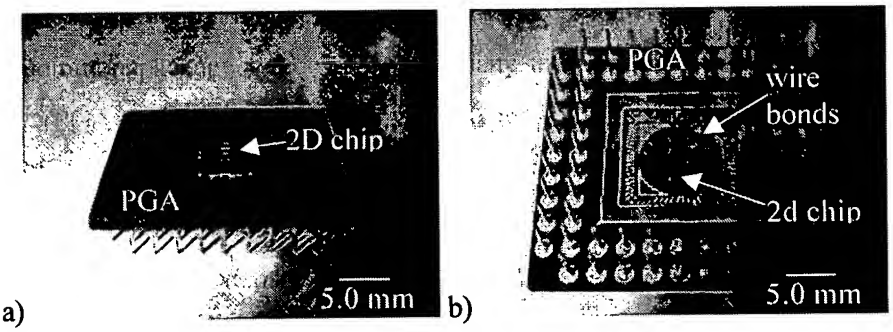


Figure 4-13. Optical image of a 2D chip in a PGA package viewed from a) the chip side and b) the pin side.

4.3. Characterization

The sensitivity and noise of the piezoresistor cantilever were studied in detail. Understanding how the ETWI affects overall performance of the cantilevers is emphasized.

4.3.1. Theoretical Sensitivity Predictions

Deflecting a piezoresistive silicon cantilever alters the physical stress of a resistor and changes its resistance. A Wheatstone bridge can be used to measure this resistance

change and measure angstrom level deflections. The layout for a typical piezoresistive cantilever is given in Figure 4-14. A voltage is used to bias reference resistors of similar resistance values as the sensor. An instrumentation amplifier is used to amplify the voltage signal. Discrete, off-chip resistors were used as references. While the reference resistors can be integrated into the silicon [85], our design chose to leave these off the chip to maximize testing flexibility.

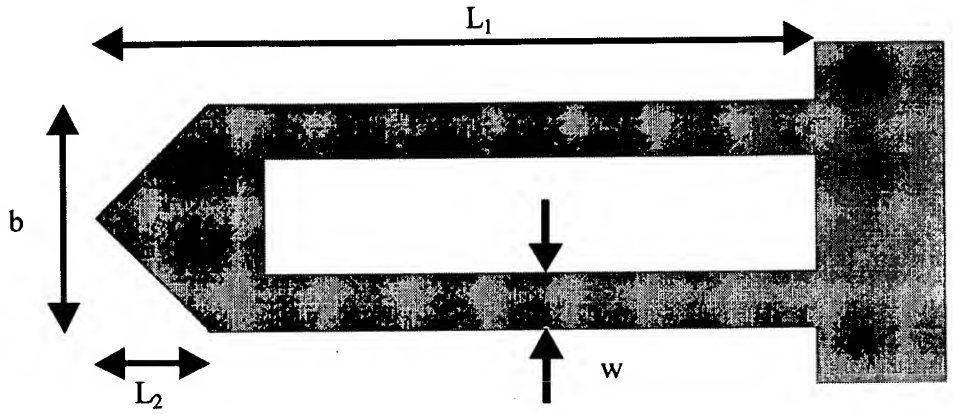


Figure 4-14. Piezoresistor cantilever dimension schematic.

A summary of the governing sensitivity equations, following Tortonese's analysis [86], is given here. The strength of the piezoresistive effect is typically expressed as a fractional change in resistivity due to the applied stress, σ. The effect is proportional to a material parameter, π the transverse piezoresistive coefficient, which depends on silicon doping and crystallographic orientation [87], giving

Equation 4-1 $$\frac{\delta\rho}{\rho} = \pi\sigma .$$

For a simple rectangular diving-board cantilever beam with width a, thickness b, and length c, the spring constant is given by

Equation 4-2 $$K = \frac{Eab^3}{4c^3},$$

where E is the Young's modulus of silicon. For the geometry of this cantilever, K is modified to allow for an isolated electrical path up one leg and back the other (Figure 4-14). The cantilever spring constant for this geometry, where t is the thickness, is

Equation 4-3 $$K = \frac{Et^3 wb}{2b(L_1^3 - L_2^3) + 6wL_2^3}.$$

The deflection sensitivity of the cantilever is typically reported as the fractional resistance change due to vertical displacement y at the tip. This assumes only the surface of the resistor responds to the stress and does not take into account nonideal dopant distributions [80]. The sensitivity is given by

Equation 4-4 $$\frac{\Delta R}{R} = \frac{3\pi Etb(L_1 + L_2)y}{4((L_1^3 - L_2^3)b + 3L_2^3 w)}.$$

Using these equations, the piezoresistive cantilevers were designed to have the properties summarized in Table 4-1. For cantilevers in the <110> crystal direction, π = 5.70×10^{-10} m^2/N and E = 1.70×10^{11} N/m^2 [87]. All calculations were done with L_2 = 60 μm, w = 40 μm, b = 120 μm and t = 7 μm.

Cantilever	L_1 [μm]	K [N/m]	ΔR/R [1/Å]
A	410	49	6.3e-7
B	350	80	8.8e-7
C	300	126	1.2e-6
D	250	218	1.8e-6
E	200	425	3.0e-6

Table 4-1. Predicted mechanical characteristics for fabricated piezoresistive cantilevers.

When a Wheatstone bridge is used to measure the change in resistance (see Figure 4-16 for an example), the voltage output V_{out}, given as a function of the gain G and bridge bias V_{bias}, is

Equation 4-5 $$V_{out} = \frac{GV_{bias}}{4}\frac{\Delta R}{R}.$$

From this equation we can see the importance of making the ETWI resistance significantly smaller than the cantilever resistance, as the ETWI resistance adds to the R in the denominator, which reduces the effective sensitivity of the sensors.

4.3.2. Measured Sensitivity

The combined series resistance of piezoresistive cantilevers and ETWI was measured when the chip was wire-bonded to a PGA package. The piezoresistive cantilever resistance alone was measured with a probe station by probing at the base of the cantilevers, before the ETWI. Both measurements resulted in the same resistance values (~1 Ω), to within the error of the measurement. Four point probe measurements of the deposited tungsten (1 μm) gave a sheet resistance of 0.1 Ω/?. Each interconnect is approximately 7 squares, giving a total resistance of less than 1 Ω/ETWI. Resistance values of each piezoresistor were consistent within each array with less than 5% variation and with a mean value of 7.5 kΩ, but were systematically 5% higher than the predicted

values. This is most likely due to inexact transfer of the cantilever dimensions. Because the ETWI resistance is much smaller than the piezoresistor resistance, it does not degrade the overall deflection sensitivity.

To experimentally measure the sensitivity of the cantilevers, the cantilevers were deflected and the voltage output of the Wheatstone bridge and its amplifiers were monitored. A feedback controlled piezoelectric actuator system with a probe needle was used to deflect the cantilever in a controlled manner. The probe displacement was linearly ramped up and down by an actuator system as the probe tip was manually brought into contact with the cantilever. Figure 4-15 is a typical deflection measurement.

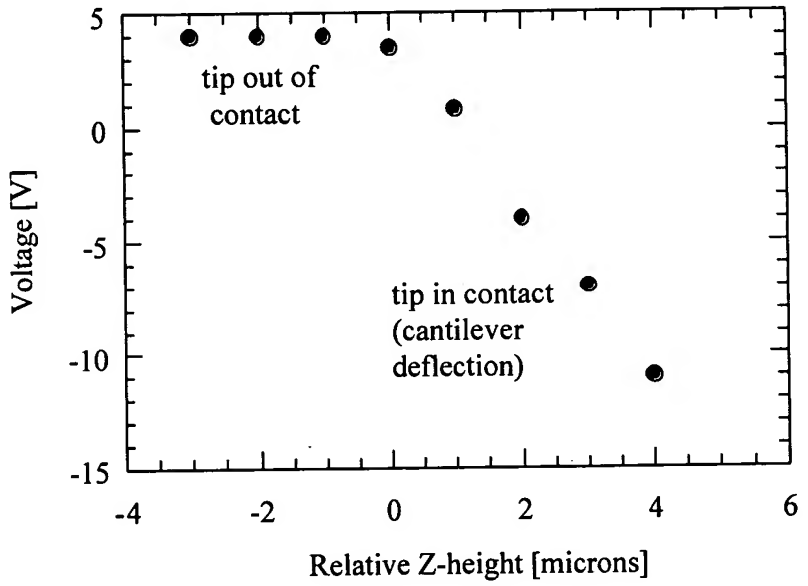


Figure 4-15. Measured Wheatstone bridge circuit output when a piezoresistive cantilever is deflected a known distance.

The ratio of bridge output voltage to deflection was measured for multiple cantilevers with dimensions A (see Table 4-1) and found to be 4.6 ± 0.05 V/μm. Solving Equation 4-5 for ΔR/R gave a measured sensitivity of 1.74×10^{-7} ΔR/R/Å, which is lower by a factor of 4 than the mask designed value of Table 4-1. SEM measurements of actual cantilever dimensions, referring to Figure 4-14, were found to be b = 106 μm, t = 6.6 μm, w = 32 μm, L_2 = 50 μm, and L_1 = 440 μm. The dimensions are smaller than intended by amounts consistent with over-exposure or over-development of the photoresist, as this

would shrink the resulting feature size. However, the cantilever length, L_1, from the base of the release region, actually increased, suggesting the backside release was misaligned. The consistency of the release, as measured by the consistency of L_1 values across the devices, was found to vary by up to 10 μm. If the HBr etch process described in Section 3.3.1 had been used, this variation may have been reduced.

Using the measured cantilever dimensions in Equation 4-4 now gives a sensitivity of 2.76×10^{-7} ΔR/R/Å which is closer to the measured value of of 1.74×10^{-7} ΔR/R/Å. These calculations assume the piezoresistor dopant profiles are box-shaped and only at the surface of the cantilever. Accounting for the nonideality of the piezoresistor doping profile further reduces the theoretical sensitivity closer to the measured value [80].

4.3.3. Theoretical Noise Sources

Characterizing the noise of a piezoresistive sensor is important because noise often limits the signal to noise ratio. Measurements and calculations were made to see if an ETWI between the sensor and amplifier increases the noise.

Two important noise sources for piezoresistive sensors are Johnson noise and low frequency (1/f) noise. Johnson noise is associated with thermally activated Brownian motion of the electrons in any conductor. It is independent of frequency, with a noise power spectral density of

Equation 4-6 $$S_v = 4KRT,$$

where R is the resistance [Ω], T the temperature [K], and K Boltzmann's constant. For a 10 kΩ resistor at room temperature the Johnson noise is 100 nV^2/Hz.

For piezoresistive sensors working in the low-frequency regime (less than 10 kHz), Johnson noise is often dominated by flicker, or 1/f noise. Defects and impurities in the bulk or the surface create traps that modulate a physical parameter such as the number of free carriers, mobility or barrier height. These fluctuations are observable when a current is driven through the resistor and have a magnitude which scales as $1/f^{\gamma}$, where γ typically varies between 0.7-1.3 [88]. In practice, the magnitude of the noise changes

dramatically with processing conditions, so it is important to measure if the ETWI process negatively affects the flicker noise characteristics of the scanning probe piezoresistors.

Other fundamental noise sources exist, but they are not generally observable with piezoresistive sensors. The unexcited resonance of the mechanical response of a vibrating cantilever is normally masked by other noise sources; only once has it been observed in air [89]. Shot noise, associated with carrier transport across a potential barrier, is a white noise source which is generally negligible in silicon piezosensors [88].

4.3.4. Noise Measurements

The Wheatstone bridge circuit in Figure 4-16 was used to measure the piezoresistor noise. The circuit used battery power with a voltage regulator to generate a stable bias free of 60 Hz line noise. Devices mounted in PGA chips were placed inside a quarter inch thick, grounded aluminum box, to shield from environmental noise (see Figure 5-35). A metal film resistor of the same resistance as the cantilever was used as a reference. The amplified signal was measured with a spectrum analyzer (HP4550). Upon biasing a device, the noise is initially high and then starts to settle (after 15-30 min) to a stable value. At this point signals were averaged to reduce random noise and the data were recorded.

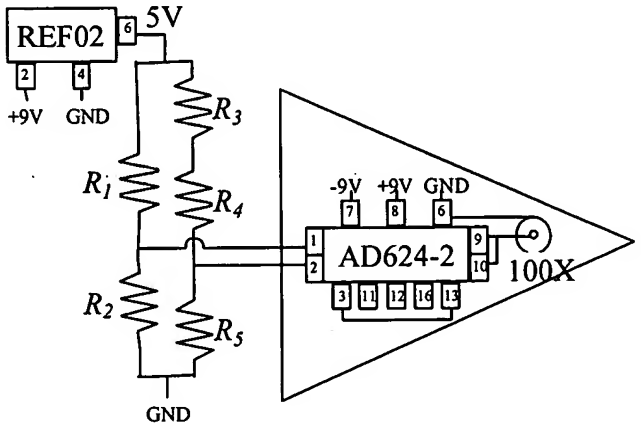


Figure 4-16. Noise measurement bridge circuit. R_1 and R_4 were typically 500 Ω resistors, R_3 a variable resistor for balancing the bridge, R_2 the metal film balance resistor, and R_5 the device under test. An instrumental amplifier set for 100× amplified the signal for the spectrum analzyer. Drawing courtesy of Yiching Liang.

A typical noise spectrum of a cantilever and its two interconnects (one for each leg) is given in Figure 4-17. The noise decreases from 100 nV/$\sqrt{Hz}$ at low frequency to a plateau of about 20 nV/$\sqrt{Hz}$ at 250 Hz. A metal film resistor of the same resistance as the cantilever (7.5 kΩ) is measured in place of the cantilever to determine the electronics noise floor, as metal resistors should have minimal flicker noise compared to a semiconductor. The two curves are nearly identical, suggesting the noise of the cantilever and its two ETWI are at the electrical system noise floor.

The electrical system noise floor consists of the sum of the noise contributions from the balance resistors and the amplifier. Noise approximately proportional to 1/f from the amplifier and metal film reference resistors dominate the low frequency noise. The frequency independent Johnson noise can be calculated by summing the noise power spectral density of each resistor in the bridge, which gives 280 × 10^{-18} V^2/Hz. Theoretically, the amplifier has a 16 × 10^{-18} V^2/Hz noise floor at 10 Hz and up to its gain roll-off frequency. The amplifier and resistor total noise spectral density is thus 17 nV/$\sqrt{Hz}$, close to the 20 nV/$\sqrt{Hz}$ floor measured.

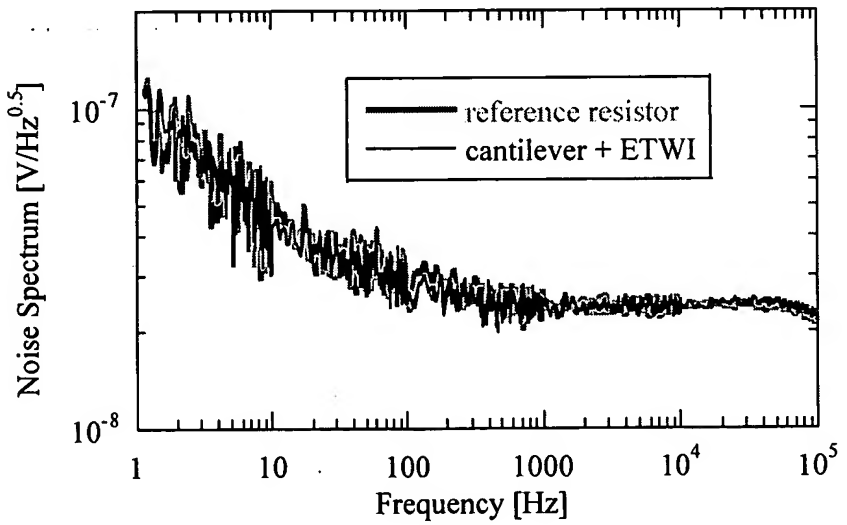


Figure 4-17. Noise of bonded cantilever and interconnect compared to thin film reference. The two curves are nearly identical.

The actual noise level of the sensor is either at or below the reference resistor noise. This level compares well to flicker noise levels reported in the literature [90]. Increasing the voltage bias (Figure 4-18) is generally associated with increased noise [91], but all measured biases appeared to be at or below the measurement noise floor.

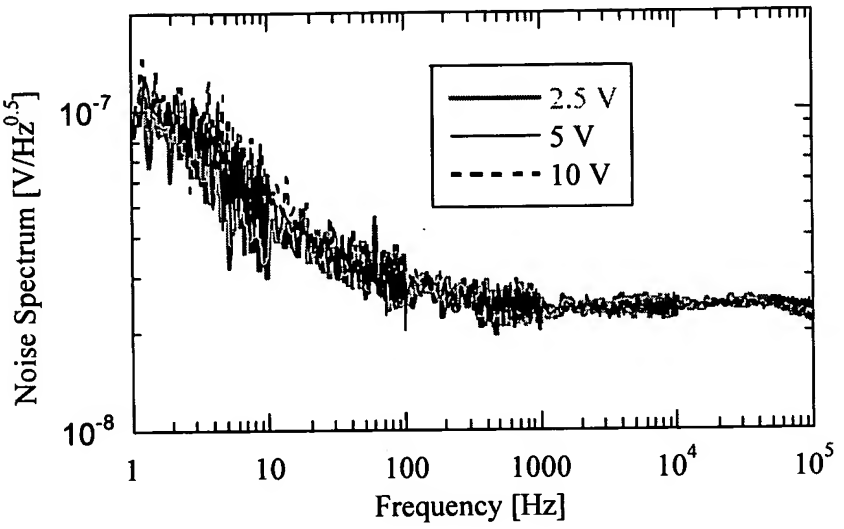


Figure 4-18. Noise as a function of bridge bias for a 7.5 kΩ cantilever and interconnect.

To characterize the noise contribution of the ETWI, the noise of a cantilever alone was compared to the noise of a cantilever plus ETWI system. The cantilever alone measurement used a probe station which required cables to reach the amplifier. This resulted in increased 60 Hz noise, but the noise floor remained the same as the other noise measurements (Figure 4-19). This suggests that the tungsten ETWI noise is significantly less than the cantilever noise. This was expected because the resistance of the ETWI is much less than the piezoresistor. It is important to confirm that plasma damage or poor metal to semiconductor contacts did not lead to excessive flicker noise [88].

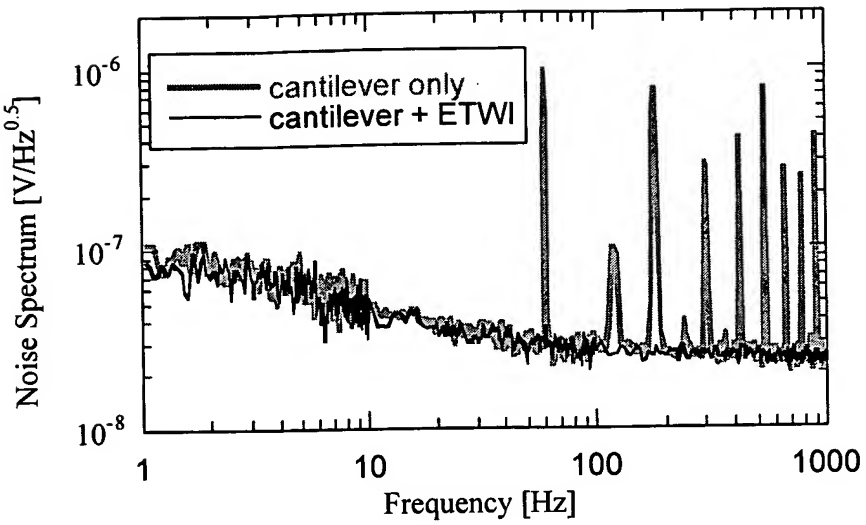


Figure 4-19. Comparison of the noise of a cantilever and its ETWI to that of a cantilever alone. Increased environmental noise (60 Hz harmonics) is observed when the cantilever alone is electrically probed with a probe station onto the frontside piezoresistive contacts.

The minimum displacement resolution can be calculated with the measured noise and sensitivity. In a 10–1000 Hz bandwidth, the integrated noise is 2.5×10^{-5} V_{rms}. Dividing this by the voltage sensitivity measured in section 4.3.2, gives the displacement sensed for a signal to noise ratio of one: 5 Å. Multiplying by the stiffness of 50 N/m gives a force resolution of 24 nN.

4.4. Scanning

To demonstrate operation of the 2D array as a microscope and the benefits of integrated ETWI, parallel contact mode scanning pictures were taken of large samples.

4.4.1. Hardware

The scanner and electronics systems are summarized here (Figure 4-20), and described in more detail by Yaraliaglu [92]. The PGA chip with the 2D array is placed in a zero insertion force (ZIF) socket mounted on the scanning head. Coaxial cable brings the signals from each piezoresistive sensor in parallel to individual Wheatstone bridge circuits, gain controls, and offset controls. Designing the electronics for amplifying and capturing this information required custom printed circuit boards and digital signal

processing chips. The amplified signals are collected by a computer with custom memory configurations.

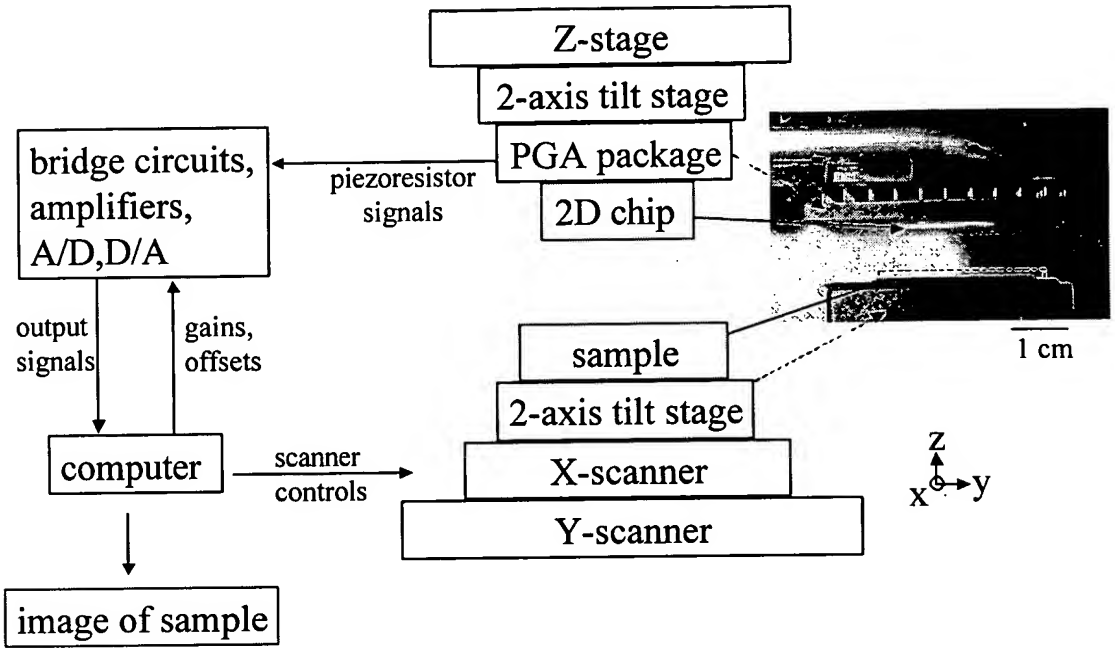


Figure 4-20. Schematic of scanning electronics and hardware.

Scanning is performed by the sample stage. A slow scanner (1-100 μm/sec) with long range (3 cm) is used to move the sample in the y-direction (Newport PM500-YK). A smaller scanner (Mad City Nano-Drive) is mounted on top of the y-scanner and is used for quickly scanning in the x-direction (up to 1 cm/sec over 200 μm). Scanning at such a high speed with minimal vertical wobble (less than 1 Å) is challenging, as the drive signal must be calibrated for each use by programming a custom digital signal processing chip.

Alignment of the 2D array to a flat sample requires aligning a one centimeter square plane to a another plane within the height of the tips (7 μm). These two planes need to also be aligned to the scan plane, so that attempting to scan does not drive the tips excessively into or away from the sample. The samples imaged were silicon wafers with thin film topography in some regions and flat, bare silicon in other regions.

To perform this alignment, we first aligned the sample stage plane to the scan plane. This was performed with a conventional single piezoresistor and a flat silicon

surface on the sample. The cantilever was mounted at an oblique angle (~10°) to the surface. The chip carrier head was vertically lowered with a micromotor until the tips were one millimeter from the silicon. A piezoelectric actuator stack, also mounted on the scan chip, was then used to carefully approach the sample until a deflection signal was observed. The slow sample stage scanner was then engaged and the amplified deflection signal observed. A two-axis gimbal stage, which rested just under the sample, was then tuned until the scan was flat in the slow scan direction (y). The fast scanner (x-direction) was then turned on, and the gimbal stage was tuned to flatten the piezosensor signal, completing the alignment of the scan plane to sample plane.

To scan with the 2D chip, the connection head for the ZIF socket must be altered so that the chip is parallel to the sample (Figure 4-21). The sample is approached with the vertical micromotor and then piezoelectric actuator. The corner cantilevers are then monitored to observe which corner touches the sample first. The 2D chip is then raised 10 μm and the appropriate gimbal is adjusted under the chip. This process of approaching, retracting, and then tuning the angle is repeated until all corner tips make contact during the same one micron vertical step. The result is that the 2D chip is vertically aligned to within one micron over a square centimeter, corresponding to an alignment accuracy of 0.1 milliradians.

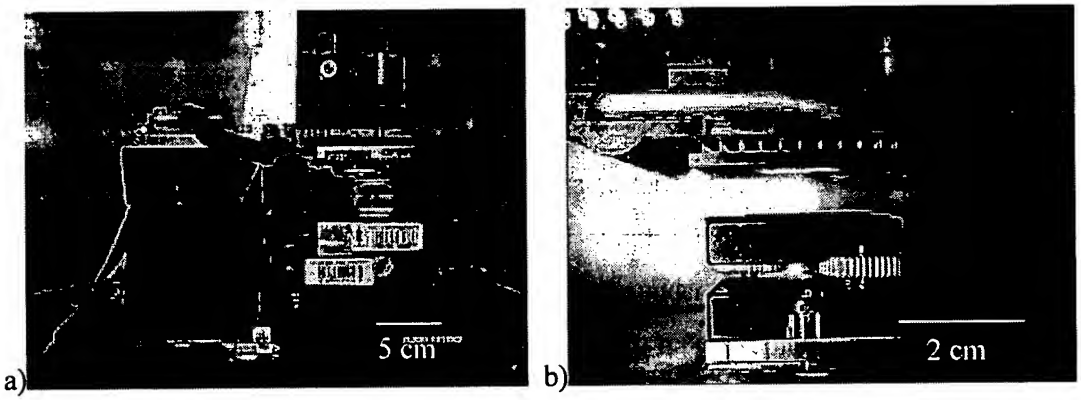


Figure 4-21. Image of scanning hardware for the 2D chip. a) Side view of mechanical scanners for movement in the Z, X and Y directions. b) Close up view of the 2D cantilever chip mounted for scanning above a sample.

4.4.2. Images

A typical parallel image is giving in Figure 4-22. Two rows of cantilevers, separated by 1500 μm are simultaneously scanned over a sample. Figure 4-23 demonstrates 15 cantilevers each simultaneously scanning 200 μm by 200 μm regions of an aluminum patterned silicon wafer, with 50 nm step height. The sample size (3 cm × 3 cm) is limited by the size of the scanner, and not by the wire-bonds of the 2D chip, as the ETWI enable scanning of arbitrarily large samples, similar to conventional single cantilever AFM imaging. To show the raw performance of the entire imaging system, the electronic images presented in this thesis are not post-processed or corrected for slopes, as is common for many published AFM images.

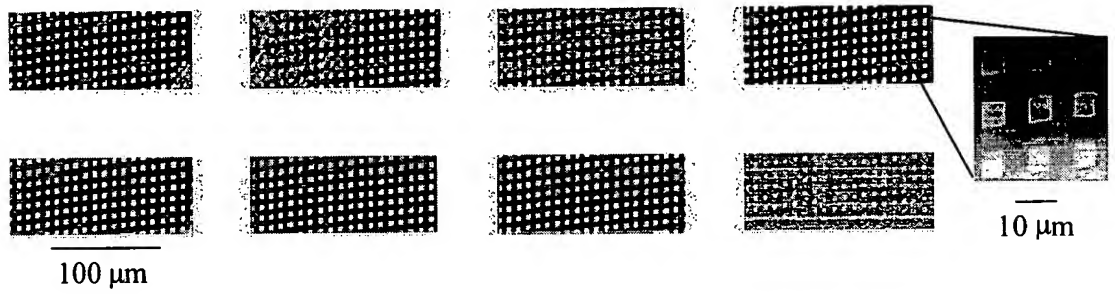


Figure 4-22. Parallel image of a grating (10 μm pitch, 0.2 μm step) with a 2 × 4 array of piezoresistive cantilevers. The cantilever pitch is 250 μm horizontally, and 1500 μm vertically. Each cantilever sweeps out a 170 μm x 70 μm area by scanning at 560 μm/sec. The entire image is scanned in 140 sec. A scratch on the grating is visible across the top left two cantilevers.

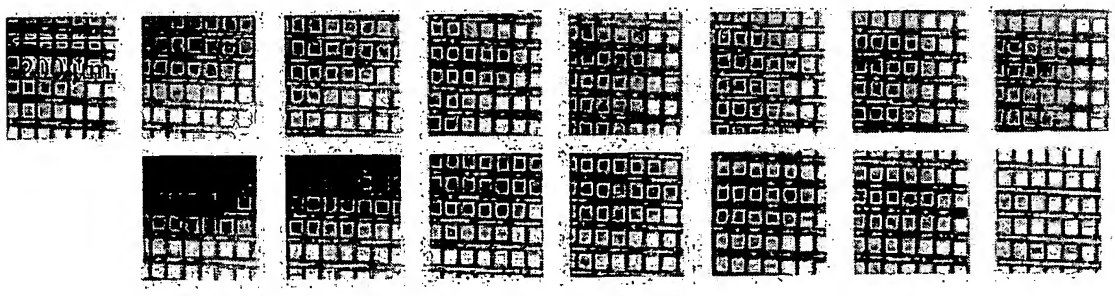


Figure 4-23. 2D parallel image with 15 cantilevers in two rows over 50 nm topography.

The required accuracy of the alignment depends on a variety of factors, including the desired contrast in the image, the size and topography of the scanning region on the sample, and the mechanical properties of the cantilever. For the images presented here, the 2D chip, sample, and scanner planes were vertically aligned to less than 1 μm over 2 cm. This planarity enabled vertical stitching of rows of cantilevers separated by 1.5 mm (Figure 4-24). The sensitivity of the cantilever combined with the parallelism of the array enables nanometer-scale sensing over millimeter-scale areas. Horizontal stitching was not possible with this particular scanner because the range was 200 μm, while the cantilever horizontal pitch was 250 μm. Due to limited computer data collection rates, there is a tradeoff between image resolution versus scan speed and range. For this image, each cantilever sweeps a 512 × 4000 pixel image in 30 minutes, with each pixel representing a 0.5 μm square.

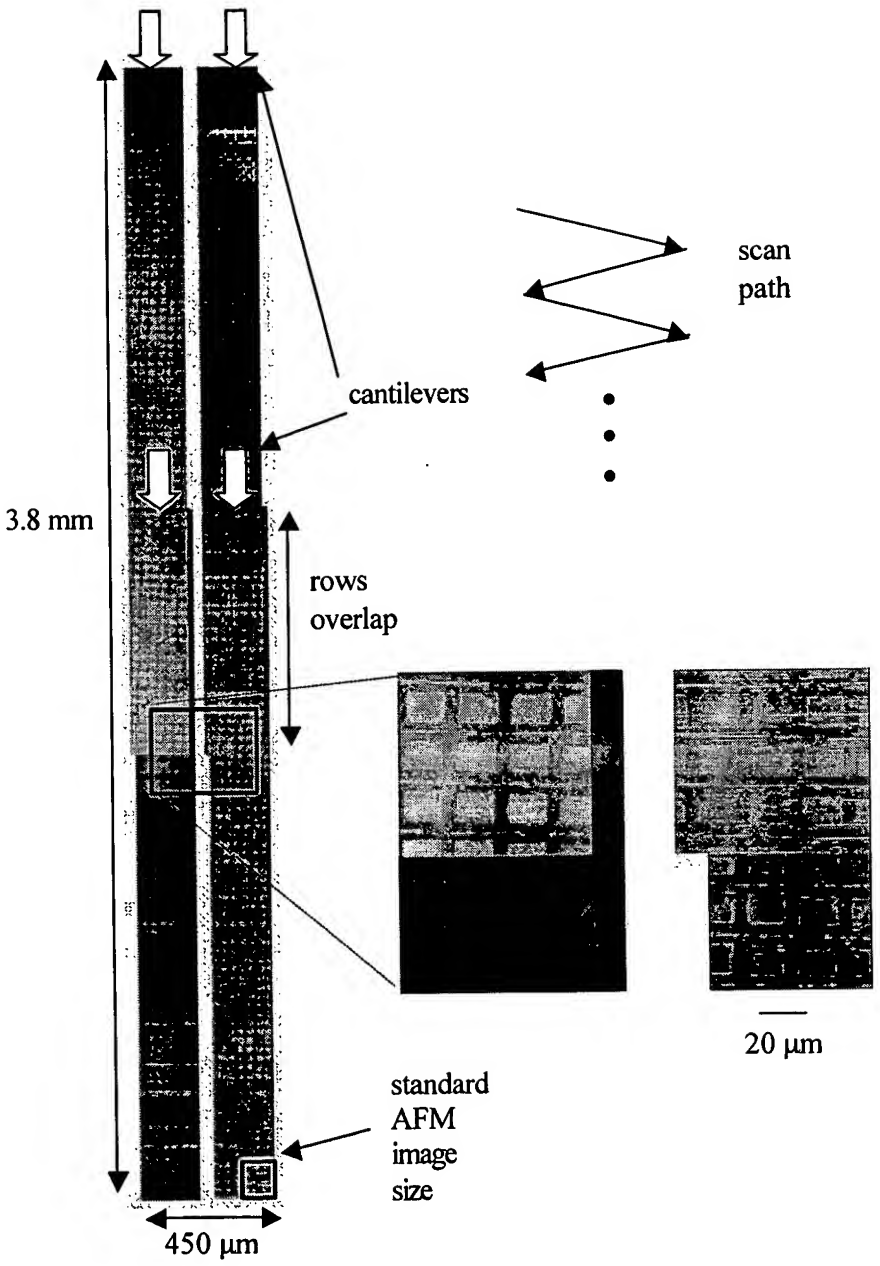


Figure 4-24. Vertically stitched parallel image from a 2 × 2 array including a full image (3.8 mm × 0.45 mm) and a close up of the vertical stitching. Topography is 50 nm tall.

4.5. Conclusion

The cantilevers were found to have quiet noise characteristics, as they were measured to be at our electronic measurement noise floor. It was not possible to distinguish between the noise of a single cantilever combined with its interconnects, and the noise of a cantilever alone, without its interconnects. Since the interconnect is metal and of low resistance (~1 Ω), it is expected to contribute minimally to the overall sensor noise. Parallel scanning of two-dimensional arrays was performed over optical gratings, demonstrating large area and high resolution capability.

Major challenges concerning scanning include alignment and tip wear. Alignment was time consuming as each sensor has to be manually aligned. Attempting to rush the process can result in crashing the scanning chip with the grating sample, which misaligns the sample to the scan plane and requires repeating the entire alignment process from the beginning. To aid in alignment, future generations could incorporate cantilevers on the far corners of the silicon chip, and not just at the corners of the cantilever array. These sensors would prevent crashes between the 2D array and the sample. If the tip heights are uniform, aligning the four corners would also align the cantilever array in the center.

However, the tip heights do not remain uniform after scanning due to tip wear. This is a general drawback of contact mode scanning microscopy, which is difficult to overcome for arrays. After fabrication, the tip height uniformity is estimated from SEM images to vary by less than 0.25 μm over each chip. However, after scanning the silicon tips on the silicon samples, wear produces height variations that lead to contrast and lateral resolution variations between the cantilevers, as seen in the vertical stitched image in Figure 4-24. Cantilevers were typically operated at a deflection of 0.5 μm to insure contact during the entire scan. This deflection corresponds to 25 μN of force for the cantilevers most often used for scanning (Table 4-1), and is within the range of forces known to induce wear for silicon-on-silicon scanning [93]. For scans over a softer material, such as photoresist, this effect would be much reduced.

Under the worst conditions, it is possible for the silicon tips to pick up dust or even break (Figure 4-25). Protecting the sample from dust helps tremendously, but the scanning process sweeps serially so all dust in the imaging region will eventually collide

with a tip. Once the dust adheres to the tip, the height and resolution of the tip is drastically changed. It is also very difficult to remove the dust due to electrostatic forces. When attempting to scan with too much force (on the order of mN) or on a sample with topography on the order of the tip height (microns), it is possible to break the tips. Unfortunately, this is a common problem with contact mode AFM scanning, which is exacerbated by the fact that this scanner is capable of speeds 10-100 times faster than normal AFM scanner speeds. Attempting to take advantage of this speed occasionally results in breaking of the tips when scanning over steps. Future designs could employ significantly wider and taller tips. Fifty micron wide tips would not reduce packing density but would significantly increase shear strength. Heights greater than 20 μm would aid alignment, but obtaining such thick silicon might require silicon bonding. Bending the cantilevers out of the plane, as demonstrated by IBM [5], is another technique which could be used to simplify scan alignment. If each cantilever had an addressable actuator, such as the kind demonstrated for linear arrays [18], than alignment as well as tip wear would be helped because feedback controlled constant force imaging could be performed with each cantilever.

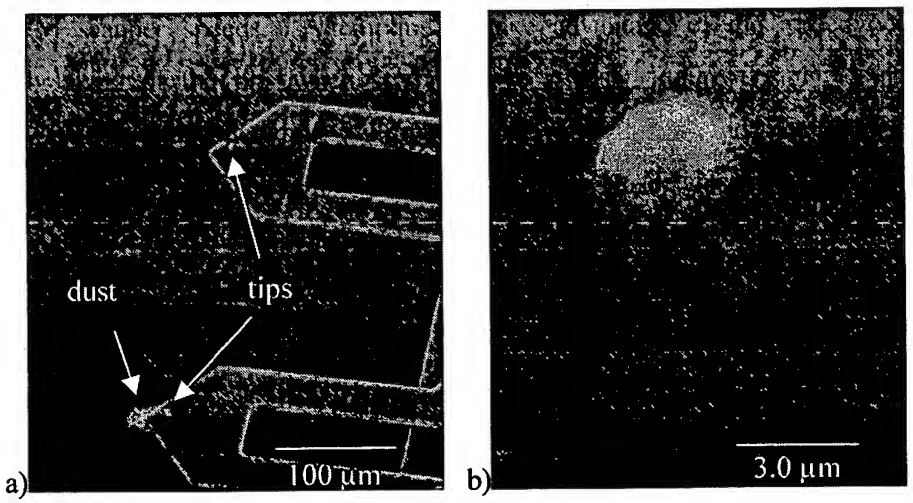


Figure 4-25. Cantilever tip wear after contact scanning. a) A tip has picked up some dust from the sample, and b) a tip has broken off, leaving only the base.

The key fabrication issue is the ease of future processing after fabricating the through-holes for the electrical interconnect. Thick photoresist processing over the holes

works well when the lithography is well aligned and the etches are short. However, the double-sided resist process over the via traps air at room pressure, which expands and ruptures resist membranes during long plasma etches. Thicker photoresists (more than 20 μm) were stronger, but much more difficult to develop without adhesion problems, and also have poor sidewalls. Mask patterns were not very alignment tolerant when over a via, as a misaligned membrane over a via is more easily torn during photoresist development (Figure 4-26). Redesigning the mask to include larger overlaps reduces the susceptibility to this problem, but at the expense of via packing density.

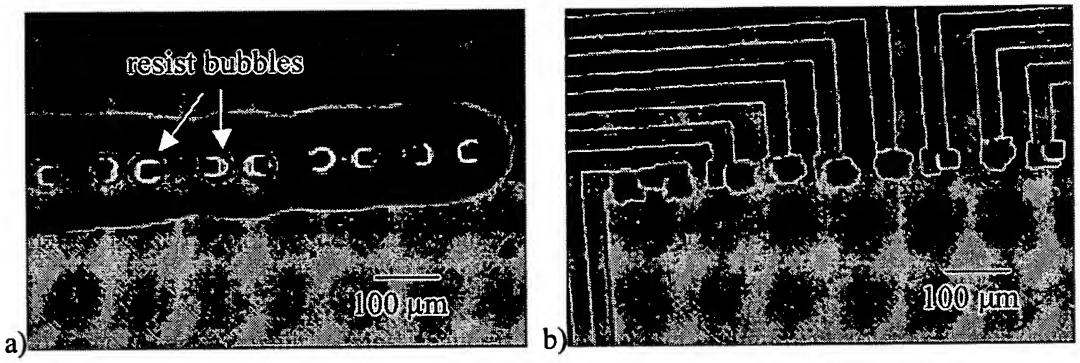


Figure 4-26. Resist mask failing over unfilled vias after a) a long plasma etch (greater than 30 min), and b) after lithography.

The photoresist mask rupture during the plasma etch caused loss of yield, as it occurred during the release etch late in the process. The thin films of the ETWI were immediately etched when the resist burst during the process, so the devices were immediately lost. Developing an interconnect which is easier to integrate with sensors is the focus of the next chapter.

Chapter 5: Polysilicon Plug Electrical Through-Wafer Interconnects

The fabrication and characterization of high-density electrical through-wafer interconnects (ETWI) on silicon substrates are described. Compared to the ETWI described in the previous chapter, these interconnects are significantly easier to integrate with existing device processes. The process uses high-temperature compatible materials and results in a filled via, making it compatible with standard semiconductor processing and wafer-handling equipment. TMICP etching from both sides of the wafer and polysilicon filling are used to form an interconnect with resistance of 10-14 Ω and capacitance of less than 1 pF, sufficient for many sensor applications. Versions with n+ type or p-type conduction, and with integrated shielding are fabricated, characterized, and modeled.

5.1. Pre-Process Integrable ETWI

As described in Chapter 1, ETWI have significant applications in integrated circuits and MEMS. This work targets ETWI applications for integration with released sensors, such as micromachined scanning probe arrays for applications in imaging, data storage, and lithography. These sensors are delicate, freestanding structures on which it is difficult to perform photoresist-based lithography, so ETWI fabrication prior to device

fabrication is preferred. This pre-process approach is in contrast to the post-process approach that many are pursuing for IC applications. In a post-process approach, the ETWI fabrication is performed after the IC or sensor fabrication, which generally limits ETWI processing temperatures and materials. See Chapter 1 for examples of post-process ETWI work.

The previous chapter demonstrated a pre-process ETWI based on tungsten that was integrated with a high-density sensor array process. The ETWI process followed fabrication of the tips, but preceded the cantilever fabrication and release, making it a pre-process. While successful, overall process yield was reduced by the many complications caused by the vias being unfilled. The process used to fabricate the scanning probes, in particular the lithography steps, needed significant alteration to accommodate the ETWI. Very thick spin-on photoresist was used to mask over the unfilled vias. This mask performed well for short plasma etches, but failed to protect the ETWI during long plasma etches because of resist bubbles. The use of thick photoresist also severely increases the minimum lithography feature size because thicker resist films are more difficult to pattern with high resolution.

This chapter introduces a pre-process ETWI based on a passively isolated through-wafer polysilicon plug. The approach pushes the limits of plasma etching to etch the smallest via possible through a silicon substrate. The substrate is a 4-inch diameter wafer that needs to remain at least 400 μm thick to be strong enough to withstand subsequent processing. A small footprint via is necessary for sensor array applications because it is important for the ETWI footprint to be significantly smaller than the sensor size. This insures that ultimate device packing density in an array, important for throughput as described in Chapter 1, is not limited by the ETWI. The devices in the previous chapter, as well as previous work in imaging, data storage, and lithography, have cantilever dimensions of the order 100 μm × 200 μm or larger. The ETWI for these applications would require a footprint area significantly smaller than this. In addition, if the via is small enough, it is possible to fill it with conformally deposited thin films, such as silicon dioxide and polysilicon. These are standard semiconductor materials that are compatible with later high-temperature processing. After filling the vias, the wafer can be handled with standard vacuum-based wafer handling equipment. If the wafer is

sufficiently planar, standard spin-on photoresist can be used for high-resolution lithography.

Such a via can dramatically facilitate ETWI integration. A wafer with these pre-processed ETWI would be ready for almost any device process without having to make significant changes to the previously developed recipe. As described below, the ability to make p-type or n-type ETWI adds design flexibility, as it is simpler to integrate p-type ETWI with p-type sensors and n-type ETWI with n-type sensors. Furthermore, a ground shield can protect sensitive signals from substrate noise and permit increased integration of different devices. The resources expended to develop a successful single ETWI device could readily be leveraged to fabricate arrays. New possibilities for integrating circuits with MEMS are facilitated, as a sufficiently planar wafer would be compatible with standard integrated circuit fabrication.

5.1.1. ETWI Design

While the required characteristics of an ETWI vary with application, for the applications this ETWI is designed for, resistance, capacitance, and footprint area are the primary design criteria of interest. For connecting to piezoresistive sensors, the ETWI resistance is the most important criteria. It should be much less than the resistance of the piezoresistor, which is typically on the order of a kilo-ohm, so as not to reduce deflection sensitivity. In addition, because low-frequency noise in piezoresistors often limits sensitivity, it is important for the low-frequency noise of the ETWI to be lower than that of the piezoresistive sensor. For connecting to a capacitor sensor, the capacitance of the ETWI to the neighboring substrate should be significantly smaller than that of the sensor. This ETWI is also to be used for a capacitor transducer array for ultrasound applications, where the required ETWI capacitance is less than one picofarad (see Chapter 6). The capacitor sensors are hundreds of microns on a side, like the cantilevers, so ETWI footprint dimensions smaller than this are desired.

To predict ETWI resistance values, the ETWI is modeled as a cylindrical conductor (Figure 5-1). The resistivity is then given as

Equation 5-1 $$R = \rho \frac{L}{A},$$

where ρ is the polysilicon resistivity, L the length of the ETWI, $A = \pi r_c^2$ the cross-sectional area, and r_c the radius of the conducting core. To minimize the resistance, the area can be increased, but this increases the footprint and makes filling more difficult. Using a conduction material with a low resistivity allows lower ETWI resistance without compromising packing density.

The conduction material must be high-temperature compatible, conformal, capable of filling the via, and sufficiently conductive. Chemical vapor deposition (CVD) techniques can be extremely conformal, because they can have very low sticking coefficients and long mean free paths compared to the dimensions of the hole. This means the probability of depositing a molecule on the surface is very low, so it takes many collisions with the surface to eventually react and adhere. Surfaces in a deep hole are thus just as likely to be deposited as a top surface. CVD tungsten and doped CVD polysilicon are two conductors that are very conformal and also high-temperature compatible. CVD tungsten, which was used in the ETWI of the previous chapter, is a refractory metal with one of the highest metal melting points (greater than 3000°C) of any metal. However, material stresses limit the deposited thickness to approximately 1 μm. For this thickness, we have measured a resistance of 0.1 Ω/?, which corresponds to 10 μΩ-cm resistivity.

In contrast, CVD polysilicon can be doped to a variety of resistance values and deposited as a film many microns thick. It is high temperature compatible, as long as a shallow doping profile is not required. For low resistance ETWI applications, a deep doping profile is required to maximize conductivity. It is possible to heavily dope polysilicon to achieve resistivity values only about an order magnitude greater than typical values for metals. For n-type phosphorus doped polysilicon, the maximum density of electrically active carriers is 1×10^{21} cm^{-3} and the minimum resistivity is 400 μΩ-cm. For p-type boron doped polysilicon, the maximum density of electrically active carriers is 2×10^{20} cm^{-3} and the minimum resistivity is 2000 μΩ-cm [94]. Arbitrarily low

resistivities are not possible because adding more doping impurities increases scattering and reduces mobility.

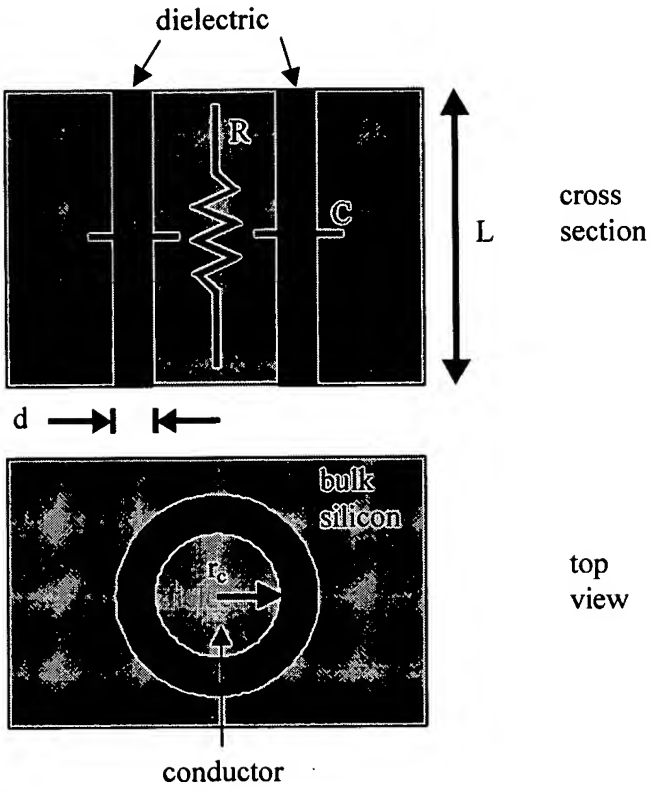


Figure 5-1. Geometry of a plugged ETWI with passive isolation and a filled conductive core.

To aid in the selection of design parameters, the capacitance can be modeled as two concentric conductors separated by a dielectric (Figure 5-1). This is the geometry of a coaxial transmission, which has a capacitance of

Equation 5-2 $$C = \frac{2\pi\varepsilon_d\varepsilon_o L}{\ln\left(\frac{r_c + d}{r_c}\right)},$$

where d is the thickness of the dielectric, ε_d the relative dielectric permittivity of the dielectric, and ε_o the dielectric permittivity of free space [95]. The actual capacitance could be lower, depending on the bias across the capacitor, because depleting the carriers in the semiconductor substrate adds a series capacitor. Thus this is a conservative estimate. While the resistance decreases for increasing radius, capacitance increases as the radius increases. Selecting a material with a low dielectric permittivity and a high thickness also helps to reduce capacitance. Thermally grown silicon dioxide is conformal, high-temperature compatible, and has a relative permittivity of 3.9, but is limited to a thickness of about 2 μm. This is because oxide growth requires diffusion through the grown oxide, which becomes more difficult as the film gets thicker. A deposited thin film such as CVD silicon nitride is also very conformal and high-temperature compatible, however its relative dielectric permittivity is nearly twice that of oxide.

Note that the polysilicon core, and the substrate silicon, can be considered good conductors for frequencies significantly less than the free charge relaxation frequency [95], f_r, where

Equation 5-3 $$f_r = \frac{1}{\varepsilon_r \varepsilon_0 \rho},$$

ε_r is the relative dielectric permittivity of the conductor, ε_0 the dielectric permittivity of free space, and ρ the resistivity of the conductor. For a silicon substrate of $\rho = 20$ Ω-cm with $\varepsilon_r = 11.7$, f_r is 50 GHz, suggesting the capacitance calculation approximation should be accurate for frequencies up to many megahertz. Similarly, the resistance calculation assumes the skin effect is negligible. This is reasonable when the skin depth distance, δ, is much greater than the thickness of the conductor. Skin depth for a good conductor can be approximated as [95],

Equation 5-4 $$\delta = \left(\frac{\rho}{\pi f \mu}\right)^{0.5}$$

where f is the frequency and μ the permeability. At 1 MHz, δ is over 1000 μm for n-type and p-type polysilicon and is 150 μm for tungsten. This design is restricted to a film thickness of a few microns so neglecting the skin effect is appropriate for up to one megahertz.

To see the ETWI electrical design space we plot the resistance and capacitance as a function of via radius in Figure 5-2, using Equation 5-1 and Equation 5-2. The length of the ETWI is set to 400 μm, the thickness of a 4-inch wafer that is strong enough for future processing. For polysilicon ETWI, the via is assumed to be filled with the maximum conducting polysilicon for the given via radius. For the tungsten ETWI, the conductor thickness is restricted to 1 μm, the thickness limit due to stress. Capacitance is calculated for the case of 2 μm oxide alone, and 2 μm oxide combined with 2 μm silicon nitride.

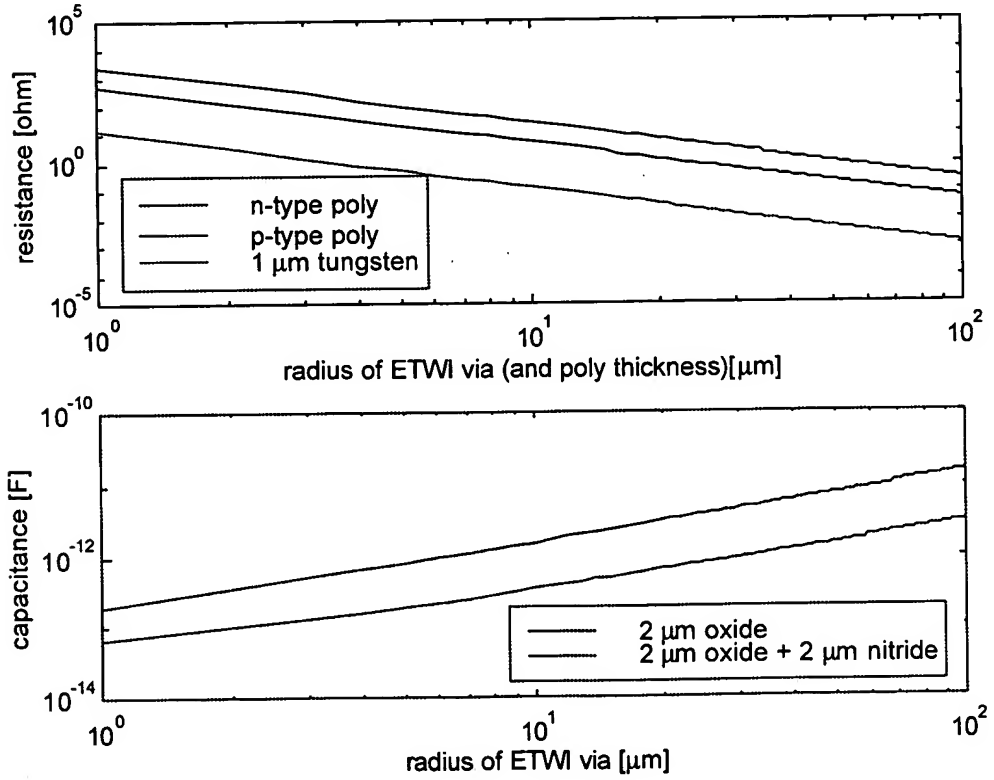


Figure 5-2. Theoretical resistance and capacitance for pre-process ETWI for a 400 μm thick silicon substrate.

A wide range of values for resistance and capacitance are possible with this geometry. Multiple design choices achieve our goal of resistance much less than 1 kΩ and capacitance less than 1 pF. Tungsten, despite being restricted to a thickness of one micron, achieves the lowest resistance. However, it is not clear how to fill the rest of the via with a conformal high-temperature material. Undoped polysilicon could be used, but Stanford does not permit tungsten in the polysilicon deposition system. An alternative is to use heavily doped polysilicon for both the conductor and the fill. For radii above 5 μm, Figure 5-2 predicts that n-type and p-type polysilicon can achieve a resistance of less than 100 Ω. The capacitance is predicted to be less than a pico-farad for radii below 20 μm. Adding the nitride reduces the capacitance by 30% compared to that of oxide alone.

This suggests that a via radius between 5 μm and 20 μm will satisfy our electrical requirements. The smaller via is preferred to minimize the footprint. However, as described in Chapter 2, plasma etching of deep vias becomes more difficult as the vias become smaller. The smallest via we can etch through a 400 μm thick wafer has a radius of 10 μm (see section 5.2.1). Thus the design selected was a 10 μm radius via, with 2 μm thermal oxide isolation, and heavily doped polysilicon conduction. This gives a predicted minimum resistance of 5 Ω (n-type) and 25 Ω (p-type), and a capacitance of 0.5 pF.

5.1.2. Shield Design

By shielding the ETWI with a driven ground plane, we can protect ETWI signals from substrate noise, reduce cross-talk between ETWI, and enable higher ETWI packing density. Piezoresistive sensors generate small voltage signals (in the μV range) that are vulnerable to external noise, especially before amplification. Potential noise sources include other actuators or circuits integrated onto the chip. For example, piezoelectric actuators have been integrated with piezoresistive scanning probe arrays to enable parallel constant force imaging [18]. However, large coupling on the order of a millivolt was added into the piezoresistor signal from the actuator drive signal. A typical drive signal for this actuator was 30 V at 7 kHz. Voltages of this magnitude or higher are common for many MEMS actuators [56]. In general, coupling to the substrate increases with voltage and frequency. Integrated circuits could also be a source of substrate noise, as digital circuits for addressing device arrays have been integrated with released

piezoresistive sensors [9]. When signals couple through the substrate, they corrupt sensitive piezoresistive signals, creating shielding challenges similar to those found in the area of mixed signal IC design.

The polysilicon ETWI designed in the previous section can be integrated with a conductive polysilicon ground shield surrounding the ETWI. Thermal oxide can be used on both sides of the ground shield for isolation between the substrate and the signal ETWI core (Figure 5-3a). The shield is made of 1 μm thick polysilicon that is heavily doped n-type to achieve a minimum resistivity of 400 μΩ-cm, similar to the signal ETWI calculation in the previous section. As the shield is a ring with radius of 10 μm, Equation 5-1 can be used to calculate a resistance of 60 Ω. The actual resistance to the driven ground pad is larger because of the connections on the surface and the bond pad, suggesting a conservative shield to ground resistance of approximately 100 Ω. The capacitance of the shield to the substrate can be calculated from Equation 5-2. For 1 μm thick thermal oxide the capacitance is 1 pF, approximately double the capacitance between the shield to signal ETWI.

To predict the effectiveness of the shielding, an analytical model was developed. This shielded ETWI is targeted for piezoresistive cantilever applications that operate at frequencies less than 100 kHz. For these frequencies, the signals have wavelengths significantly larger than the dimensions of the devices, which suggests that a lumped RC model is adequate for modeling. A substrate signal, in this approximation, would see AC circuit paths to ground through the shield and then through the ETWI (Figure 5-3b).

Solving this circuit for the ratio of V_{ETWI}/V_{sub} gives

Equation 5-5
$$\frac{V_{etwi}}{V_{sub}} = Z_1 Z_2 = \left(\frac{R_{shield}}{R_{shield} + Z_{C_{shield}}} \right) \left(\frac{\frac{1}{2} R_{etwi}}{R_{shield} \| Z_{C_{shield}} + Z_{Cetwi} + \frac{1}{2} R_{etwi}} \right)$$

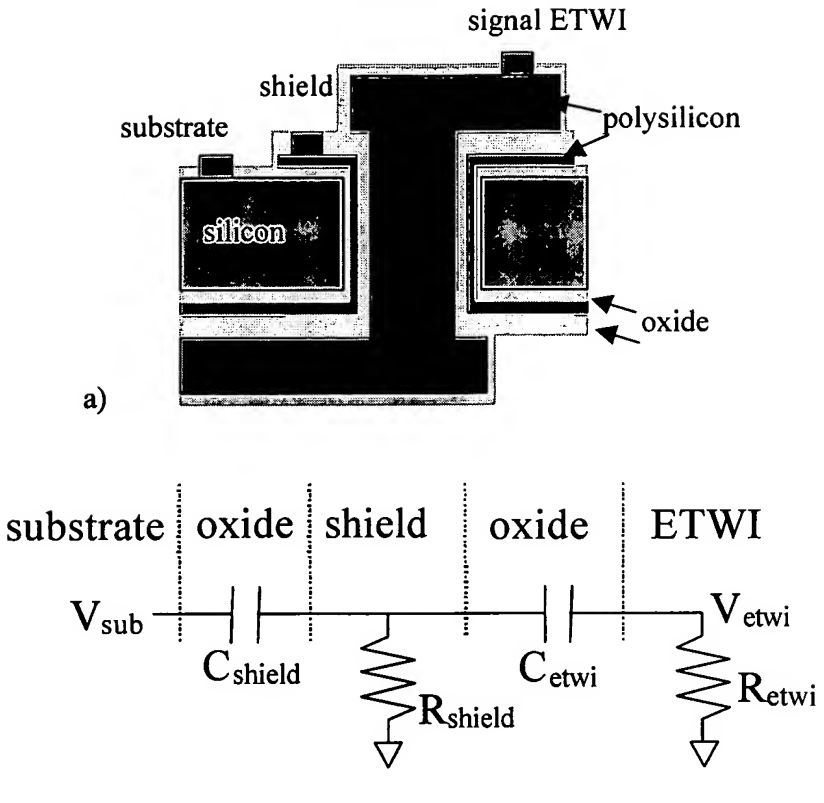


Figure 5-3. a) Polysilicon filled ETWI with integrated ground shield and b) lumped circuit AC model.

where V_{sub} is the substrate voltage, C_{shield} the shield oxide capacitance, R_{shield} the shield resistance, C_{ETWI} the ETWI oxide capacitance to the shield, V_{ETWI} the voltage on the ETWI, and R_{ETWI} the resistance of the ETWI chain. The symbol "||" is shorthand for impedances in parallel. For the case of no shield, Equation 5-5 can be used to calculate the coupling assuming R_{shield} and $Z_{Cshield}$ go to infinity. The effectiveness of the shield can then be characterized as the difference between the coupling when the shield is on and the coupling when the shield is not present. Using, R_{ETWI} = 5 Ω, C_{ETWI} = 0.5 pF, R_{shield} = 100 Ω, and C_{shield} = 1 pF, Equation 5-5 predicts that the shield will provide 100 dB of relative shielding at 10 kHz (Figure 5-4).

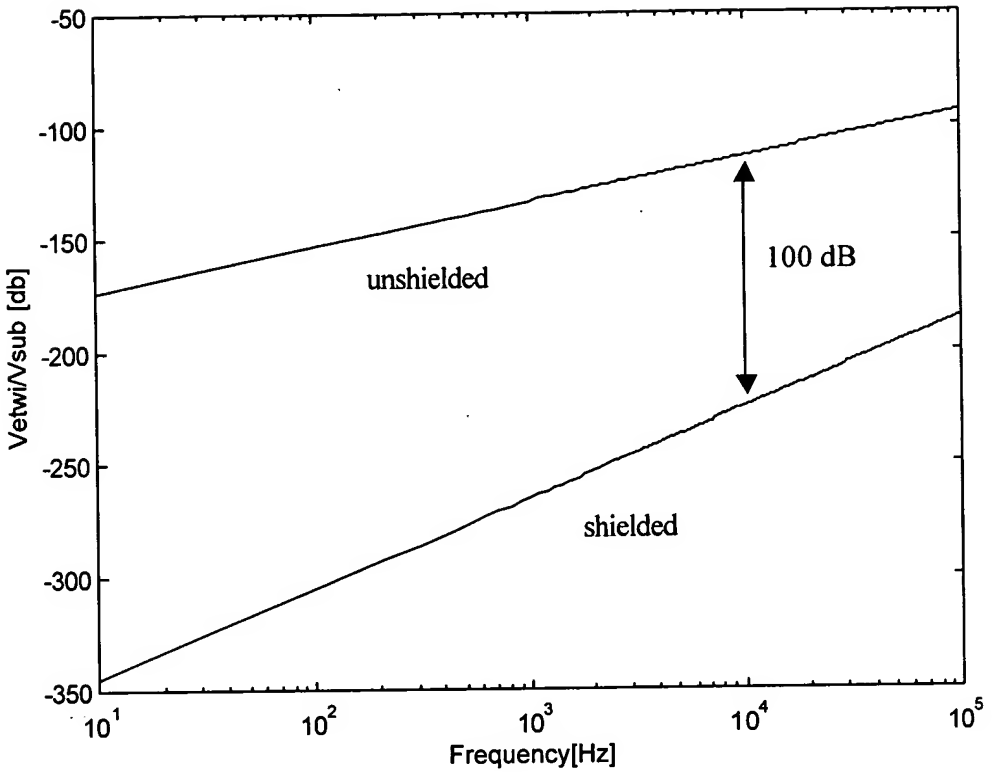


Figure 5-4. Voltage coupling between a single ETWI and the substrate, with and without a 100 Ω polysilicon ground shield.

5.2. Fabrication

The fabrication process for the polysilicon plug ETWI consists of etching a high-aspect ratio through-wafer via and subsequently coating with an insulator and then a conducting signal layer (Figure 5-5). The process requires eight lithography steps. An additional mask level and an additional conducting layer are required for a ground shield (Figure 5-6). For process details not described here, see Appendix C.

The starting substrate is a 400 μm thick double polished silicon wafer. Whether n-type or p-type wafers are used depends on the device application. For this demonstration n-type substrates with 1-20 Ω-cm resistivity were used. After scribing the wafers, global alignment marks are etched into the silicon on both sides of the wafer. Use of a backside contact mask aligner and thin photoresist (1 μm) insures good

alignment (± 1 μm) between the front and back sidse. This greatly simplifies future lithography for a double-sided process, because mask aligners do not have to be used in backside mode (which is less accurate and more difficult to integrate than simple frontside alignment).

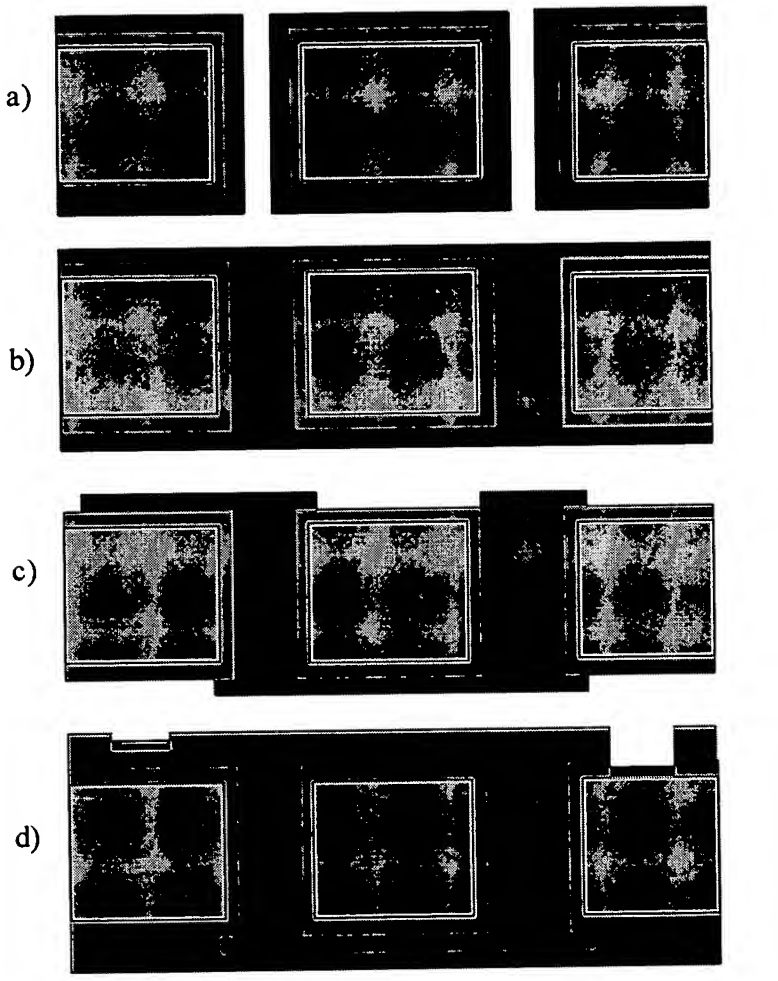


Figure 5-5. Process flow for a pre-processed ETWI without shielding. After etching the via (see Figure 5-6a-c), a) oxide and polysilicon are deposited. The polysilicon is diffusion doped, and then b) the via is filled with polysilicon. c) The polysilicon is patterned on both sides of the wafer, and then d) passivated with oxide, and aluminum contacts are formed.

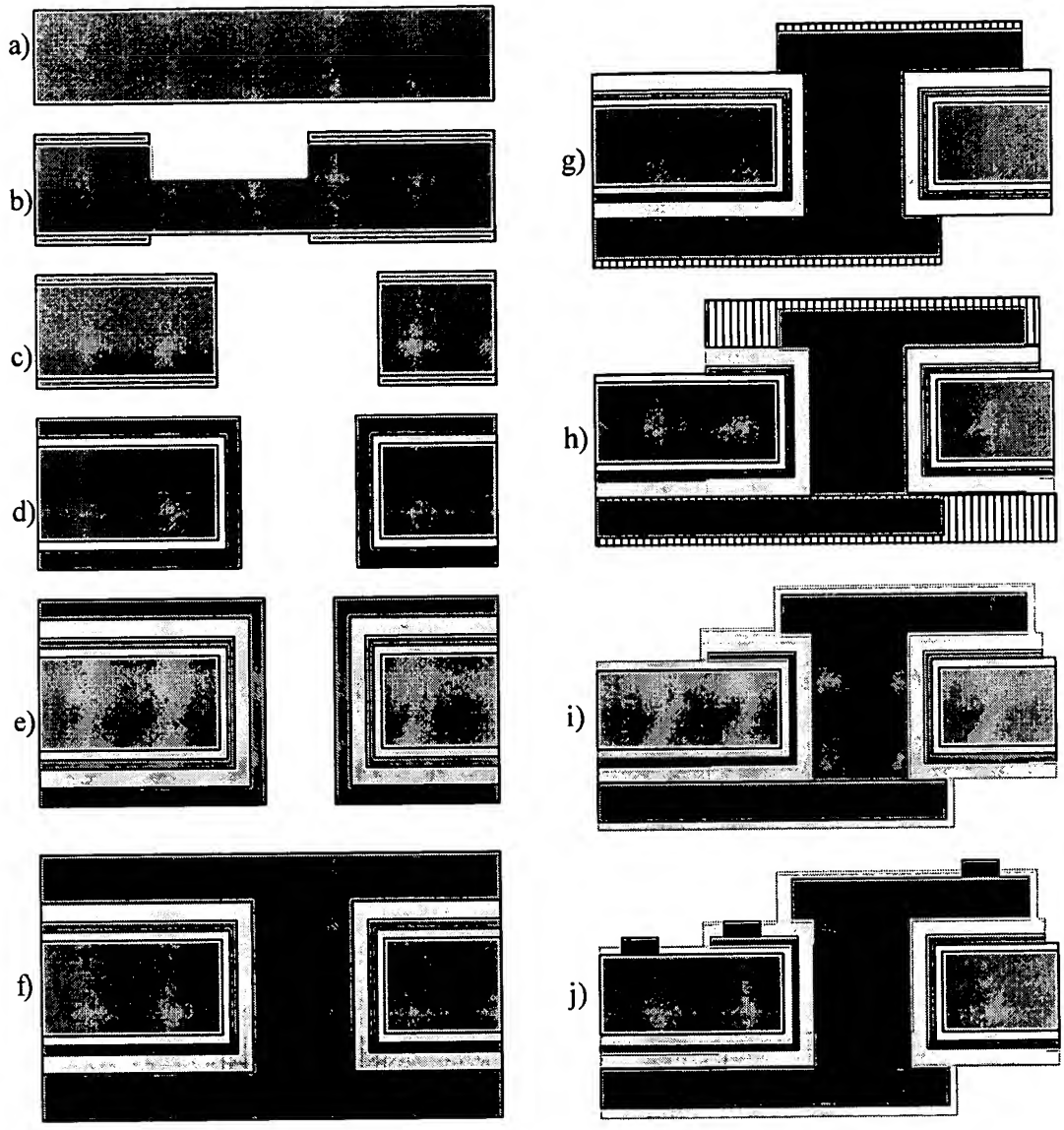


Figure 5-6. Fabrication process for a shielded pre-process through-wafer interconnect. a) Starting silicon substrate. b) Holes are etched halfway through the wafer with resist masks. c) Holes are etched from the backside of the wafer, meeting the frontside holes. d) Oxide and then polysilicon are deposited. e) Oxide and then polysilicon are deposited again for the shield. f) After diffusion doping, additional polysilicon is deposited to fill. g) Signal polysilicon is patterned. h) Shield polysilicon is patterned. i) Oxide passivation and j) contact metalization.

5.2.1. Double Sided Etching for Increased Aspect Ratio

Etches with the required aspect ratios (greater than 20:1) have been previously reported, but they are of trenches, with one dimension very long (greater than 1000 μm), or not deep enough to go through a 400 μm thick wafer [36, 55, 62]. Aspect ratio dependent etching, where smaller areas etch slower, is a characteristic of fluorine-based plasmas [96]. In our characterization of the TMICP etch process (Chapter 2), we observed that this effect is particularly severe when one dimension of the pattern is less than 100 μm. This is confirmed by our observation that trenches (20 μm x 1000 μm) take three times less time to etch 200 μm deep compared to a circle (20 μm diameter). By etching from both sides of the wafer, the average etch rate is higher, which shortens the total etch time and permits the use of thinner masks. The required aspect ratio is reduced by a factor of two from 40:1 to 20:1, and it is possible to etch a 20 μm diameter circle through a 400 μm thick wafer.

The vias can be masked with either photoresist or silicon dioxide. Ten micron thick photoresist (Shipley SPR220-7) is initially coated on one side of the wafer. After a 120 second hotplate bake at 90°C, the other side is similarly coated, and the wafer is baked in a 110°C oven for 60 minutes. Previously patterned alignment marks on the frontside silicon, combined with a backside contact mask aligner (KarlSuss), enable the exposure of aligned 20 μm circles on both sides of the wafer. The wafers then sit in air for 8 hours to absorb water. This moisture helps to ensure shorter develop times (90 seconds in Shipley LDD26W) and thus straighter resist sidewalls.

The TMICP etch is then performed from the front side of the wafer for 210 minutes, using recipe SMOODEEP described in Table 2-1. Resist is then coated and baked on the front side for use as a seal from the wafer-chuck helium gas cooling. As described in Section 1.1.4, pressurized helium is used to cool the backside of the wafers while etching. It is important for this helium to be sealed behind the wafer, so that it does not enter the plasma region. Helium in the plasma region could displace the etch and passivation gases, and disturb the RF impedance matching of the plasma. This is necessary because another 180 minute etch, this time from the backside, is then performed to punch through the via. All TMICP etching uses the wafer holder detailed in Section 3.4.

The etch is very anisotropic, and alignment is as accurate as the lithography (± 1 μm. The overetch time of the second etch, which punches through, should be minimized to reduce lateral etching of the front side silicon. Using an etch recipe with increased passivation for the final 30 minutes helps to limit this effect. Figure 5-7 depicts a completed via.

Instead of photoresist alone, one micron of thermally grown oxide can also be used as a mask. Dry or wet etching can be used to pattern the oxide with one micron photoresist. To insure against black grass (see Figure 2-11), it is important to follow a dry etch with a buffered hydrofluoric acid (BHF) dip. Then the above etching procedure can be followed. To shorten the etch time, TMICP recipe DEEP for 150 minutes can be used to replace SMOODEEP for 210 minutes. The profile for DEEP is more box-like and makes it easier to ensure a full diameter hole exists at the intersection of the frontside and backside etch (see Figure 2-10).

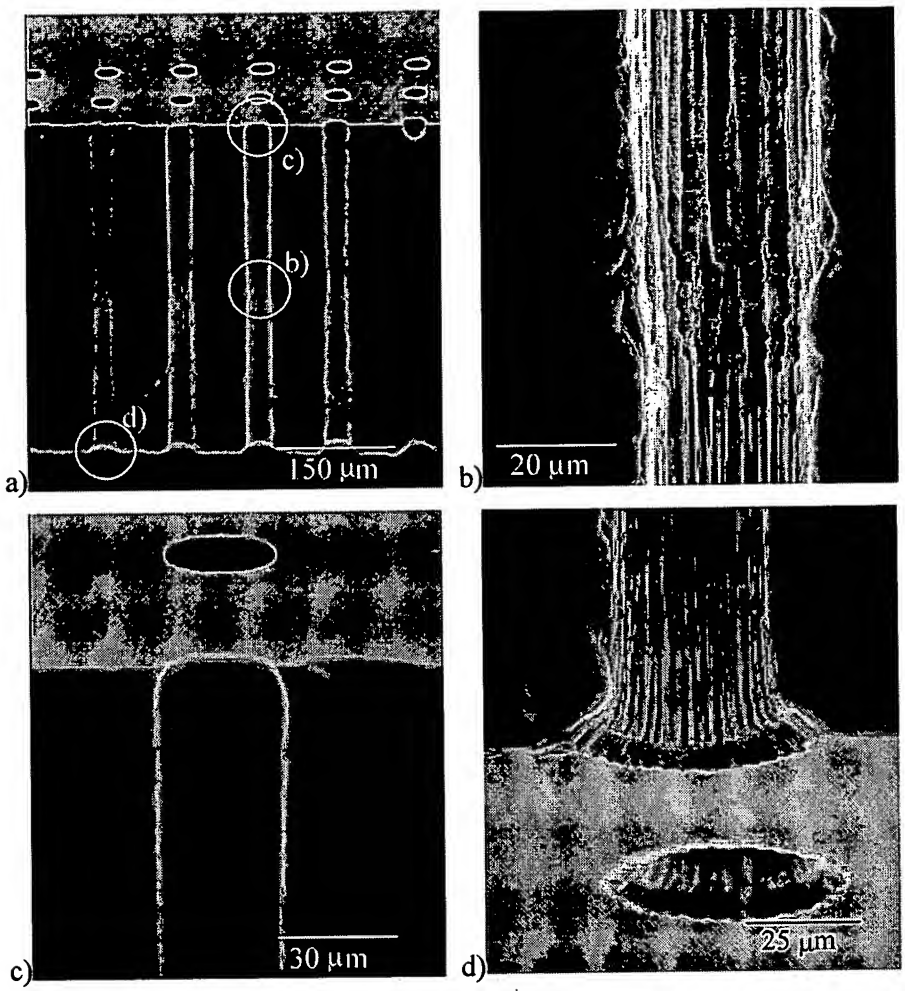


Figure 5-7. Cross sectional SEM of through-wafer via, etched from both sides of the wafer. a) Full cross section and close ups of the b) mid-section, c) top and d) bottom.

5.2.2. Filling the Via

After forming the via, conformal thin films are deposited. For electrical isolation, thermal silicon dioxide (2 μm) is grown at 1100°C. For signal conduction, low pressure chemical vapor deposition (LPCVD) polysilicon (3 μm) is deposited at 600°C. If n-type interconnects are being fabricated, this is followed by phosphorus diffusion at 1000°C for 30 minutes. A carrier gas is used to bring vapor from liquid phosphorus oxychloride ($POCl_3$) to the wafers, which combines with oxygen to deposit P_2O_5 on the wafers. If p-type interconnects are being fabricated, polysilicon deposition is followed by boron diffusion at 1000°C for 30 minutes. Similar to the phosphorus diffusion, a carrier gas brings vapor from liquid boron tribromide (BBr_3), which combines with oxygen to deposit B_2O_3 on the wafers.

The diffusion doping is followed by a BHF dip to remove the phosphosilicate glass which forms on wafers during n-type diffusion. For p-type wafers, a borosilicate glass forms during doping which is more difficult to remove. To do so, a BHF dip is performed, followed by 2500 Å wet oxidation at 1000°C. This converts the glass into an oxide that is then readily removed by another BHF dip. This cycle of polysilicon deposition, doping, and then glass cleaning, can be repeated to achieve a lower resistance. However, severely over-doping beyond the saturation limit can cause low quality polysilicon layers, forming doping rich phases that etch in BHF and create holes in the polysilicon [94]. For the n-type wafers, the doping cycle was repeated twice, and for the p-type wafers two or three times. Boron is less conductive than phosphorus so the increased doping was performed to compensate for this.

To fill the via, more LPCVD polysilicon is deposited (5-7 μm). Another 30 minute phosphorus (or boron) diffusion is performed to make the surface conducting, followed by another BHF dip, and then a 120 minute anneal at 1000°C to fully drive dopants throughout the polysilicon (see Figure 5-5b). This high temperature step, like the others, also serves to relieve stress in the thick polysilicon layers.

To add a ground shield, another oxidation must be performed, followed by doped polysilicon deposition. This is performed just before filling with polysilicon, but after the

initial oxide and polysilicon deposition (see Figure 5-6). The second thermal oxidation for the shielded case should be the thickest to minimize capacitance. If two microns are grown, about one micron of the underlying polysilicon is consumed. Since dopants diffuse quickly in polysilicon, the anneal and the oxidation drive the dopants deeper into the polysilicon, so that a conduction layer still remains after the oxide is grown. The segregation coefficient for phosphorus favors high-doping in the polysilicon, so oxidizing the doped polysilicon can lead to higher phosphorus concentrations and thus a low shield resistance.

Cross sectional images of filled vias are shown in Figure 5-8 and Figure 5-9. A 3-5 μm dimple at the entrance to the via exists. One micron photoresist adequately masks over this, but planarization techniques can also be applied if needed (see Chapter 6). An occasional ETWI exhibited a polysilicon void in this filling process, but because the ETWI are sealed under vacuum we do not expect subsequent stressing in low-pressure systems. It is however possible that the voids could contribute to absolute resistance variations, because this would change the effective electrical cross section of the resistor.

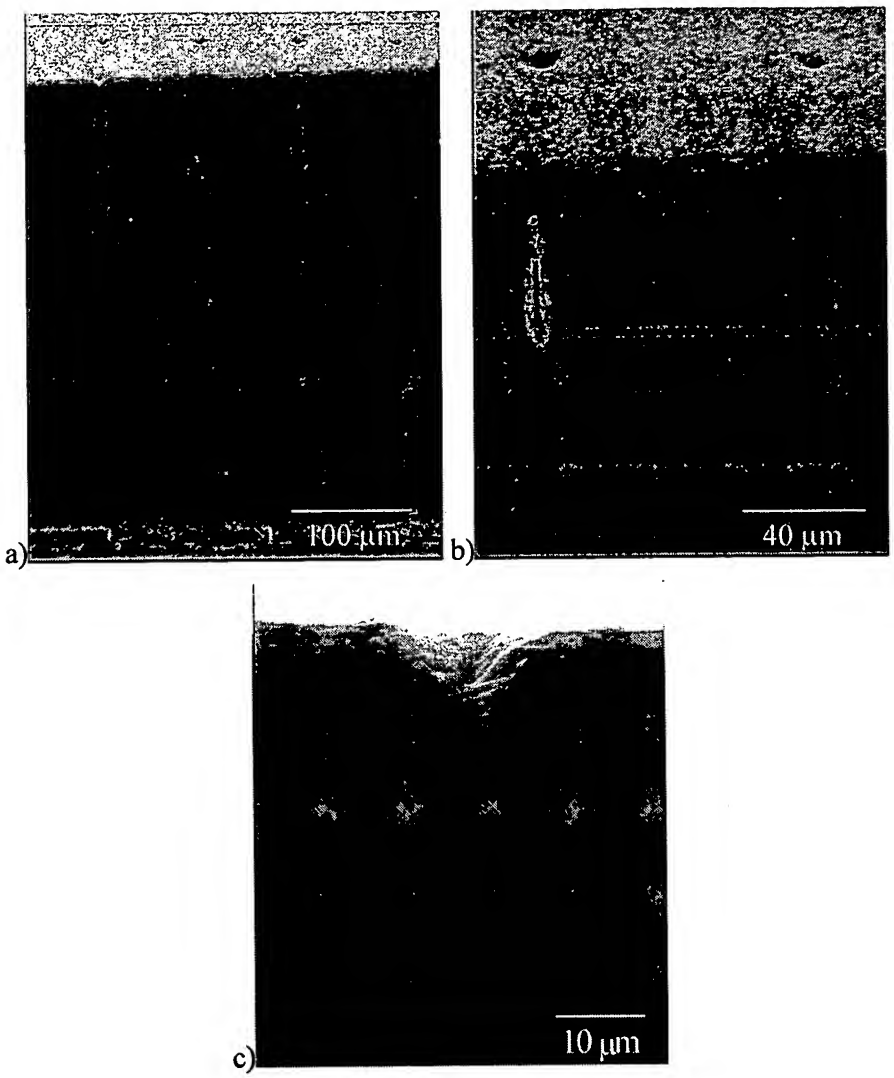


Figure 5-8. Cross-sectional views of filled vias. a) Full cross section. b) Close up of a void. c) Close up of a dimple.

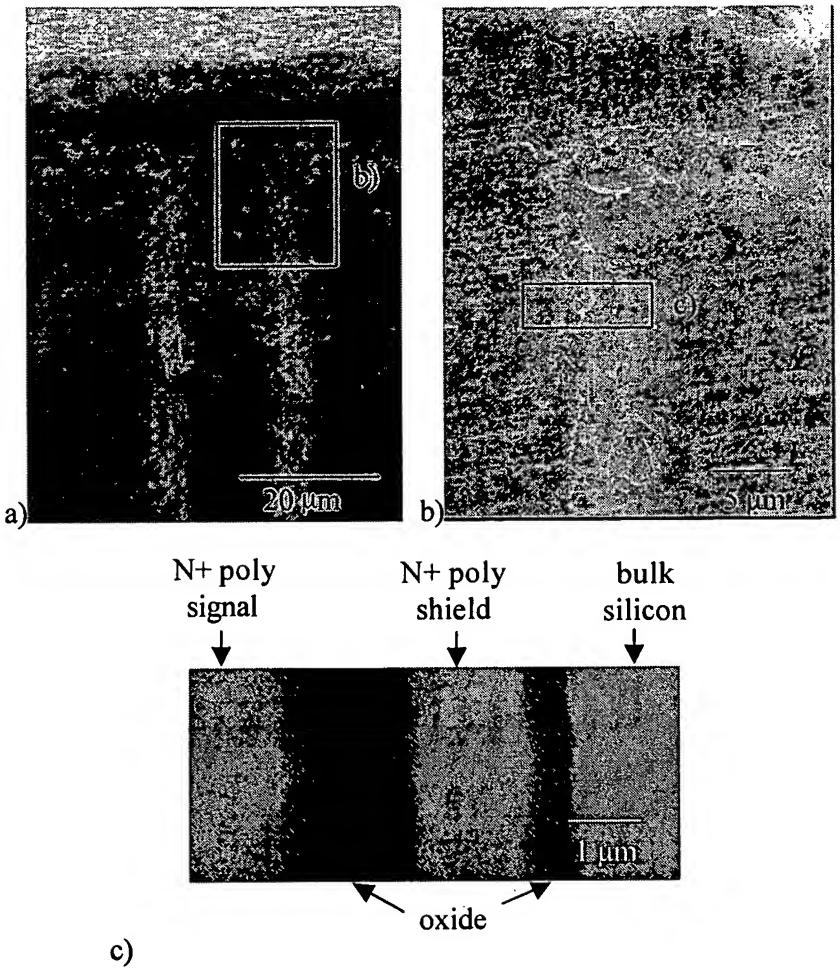


Figure 5-9. Closeups of an ETWI with a ground shield, showing the polysilicon signal and ground layers.

5.2.3. Patterning the ETWI

Because the vias are filled, we avoid the trapped air issues that arise during final patterning of the unfilled ETWI used in the 2D array (Chapter 4). To form connections to the vias, conventional spin-on photoresist is used to pattern the polysilicon with SF_6 plasma. Connections are etched on both sides of the vias, connecting the ETWI in chains (Figure 5-5c). For the ground shield case, another lithography step is used to pattern the oxide and polysilicon ground shield (Figure 5-6b).

The minimum spacing of the ETWI determines the maximum packing density. Twenty micron spacing (40 μm center to center pitch) were the densest vias designed. This spacing was at the limit of process capabilities, because of via entrance/exit overetching and lithography overlay alignment errors. As demonstrated in Figure 5-7d, the exit hole for the final TMICP through-wafer etch tended to laterally etch during overetching, expanding the diameter from 20 μm to 25 μm. This is the same kind of uncontrolled lateral etching described in Section 3.3. The designed overlay for the connection lines did not account for this. Lithographic mask alignment was also very difficult because the alignment marks were buried under 10 μm of polysilicon, so the overlay was typically ± 5 μm instead of the usual ± 1 μm. Figure 5-10 shows polysilicon connection lines that were well aligned on the front side (less lateral blow out), but poorly aligned on the back (larger blow out). Despite some of the hole being exposed and thus etched, the ETWI perform well.

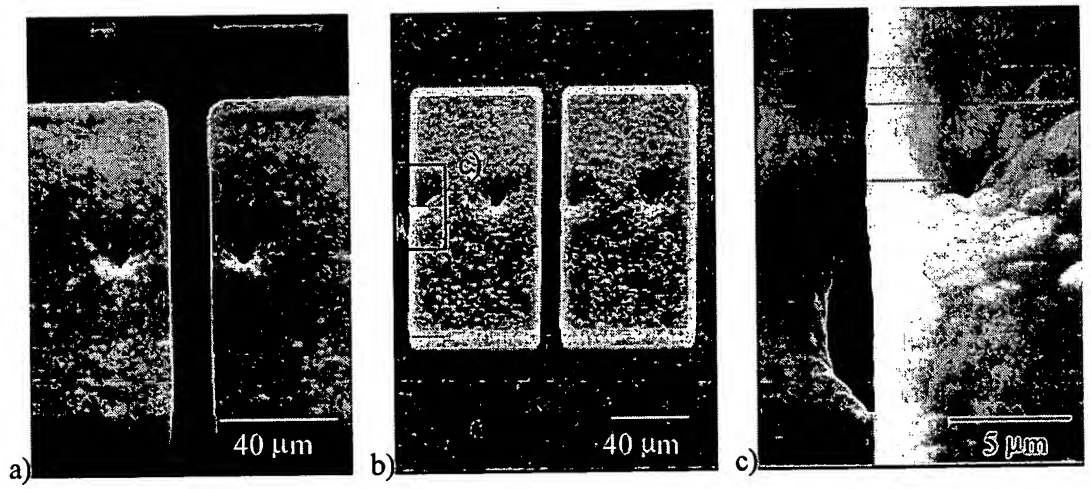


Figure 5-10. Close up of polysilicon over the vias on a) the top and b) backside of the wafer, and c) overlay lithography limits (closeup of b).

After patterning, the devices are passivated to protect the resistors from the environment and maintain isolation between the bond pads during probing. To encapsulate the devices, one micron of low temperature oxide is deposited. To make contact to the substrate, and ground shield if present, two to three microns of oxide are then patterned. With photoresist masks, this is generally very difficult to pattern with

either wet or dry etching, as these masks often have adhesion problems during long BHF etches, or overheat and crack during long oxide plasma etches. Stanford does not have a backside helium cooled oxide plasma etcher that can handle wafers with patterning on the backside. To pattern the oxide, 1000 Å of polysilicon was deposited and used as a wet etch mask. Polysilicon adheres well and did not delaminate during the 45 minute BHF etch for the contact holes. Aluminum for wire-bonding was then sputtered and patterned (Figure 5-6). Figure 5-11 shows typical ETWI chain and pad geometries.

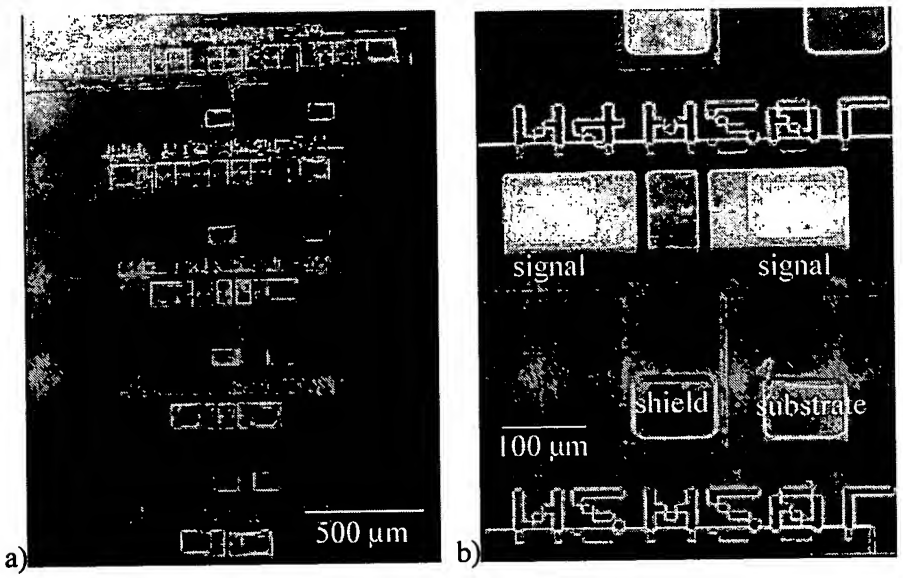


Figure 5-11. a) Top view of ETWI chains with isolated ground planes. b) Close up of a chain of four ETWI.

5.3. Electrical Characterization

In the sections below, we describe measurements that were made to characterize the electrical properties of the ETWI. Their ohmic behavior is observed and the resistance is extracted for single n-type and p-type ETWI. The resistance of the shield is then measured. The oxide capacitance of a single ETWI and its shield are extracted from chain measurements. The effectiveness of the shield is quantified through measurements of the substrate coupling to the ETWI. Finally, the noise of ETWI chains is measured.

5.3.1. IV Curves

Current versus voltage measurements were made of interconnect chains to determine the resistance of the structures and demonstrate ohmic behavior. The slope of each curve is inversely proportional to the resistance sum of the ETWI and the planar lines between them (50 μm wide, 110 μm long in this case). Measurements were taken with an HP4155A parametric analyzer.

Initial devices were probed directly with a probe station tip, as they did not have aluminum pads for wire-bonding [97]. Ohmic behavior is observed, although a slight hyperbolic sine shape is observed in the IV curves of the ETWI chains, particularly for short chains (Figure 5-12). Activation energies associated with grain boundaries have been reported to be a characteristic of polysilicon resistors, but at lower doping levels [98]. Poor probing contact or Joule heating can also cause such nonlinearities [99]. Subsequent devices were made with aluminum contacts and were also measured to be ohmic (Figure 5-13). P-type IV curves also show ohmic behavior, and are given in Figure 5-14.

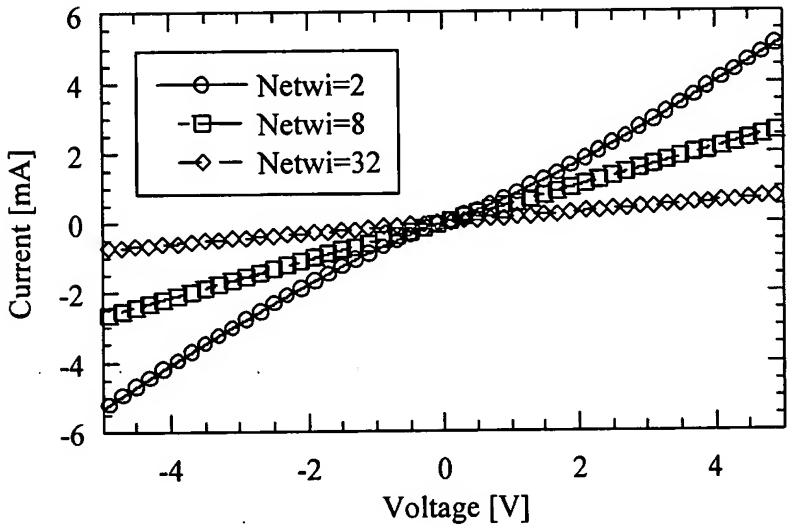


Figure 5-12. Current-voltage curves of n-type ETWI chains. The polysilicon was probed directly, as no aluminum or wire bonds were available on these devices.

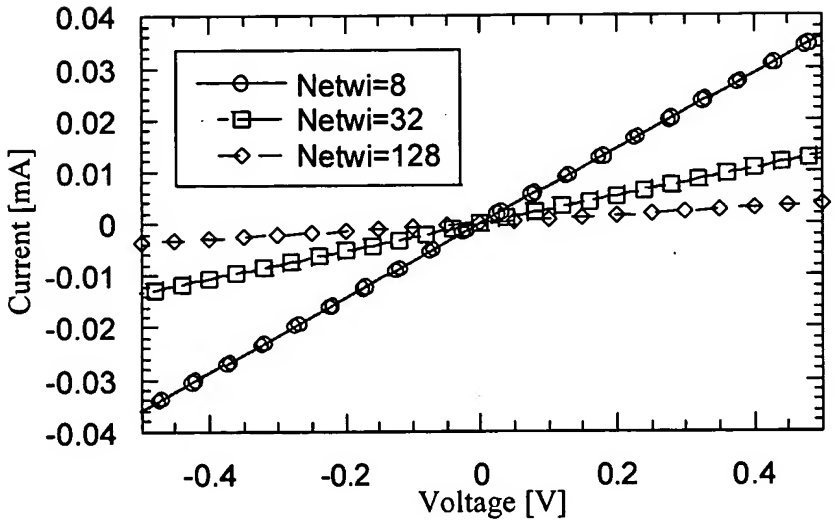


Figure 5-13. Current/voltage curves for n-type ETWI chains with aluminum bond pads.

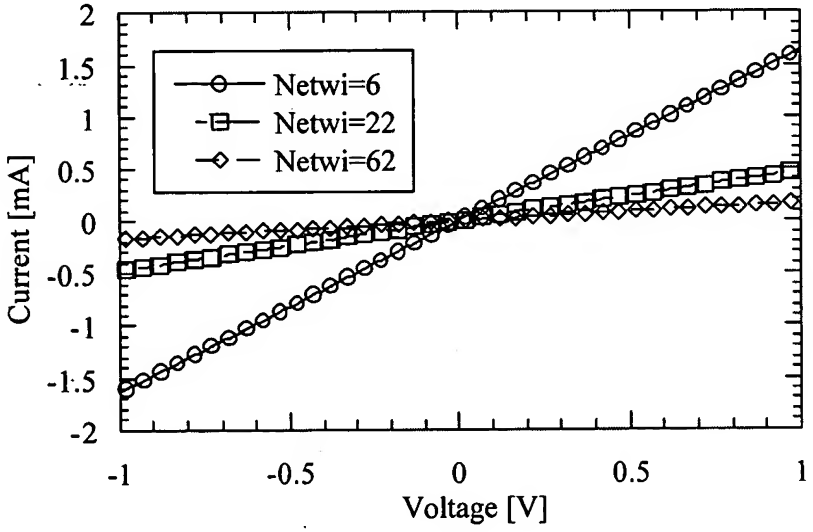


Figure 5-14. Current/voltage curves for p-type ETWI with aluminum bond pads.

5.3.2. Resistance

The resistance of a single ETWI is extracted from measurements of chains of ETWI and planar test structures (Figure 5-15). The planar test structures allow measurement of the resistance between each ETWI along the wafer surface. Chains of different lengths were measured and plotted as a function of the number of ETWI (Figure 5-16). The resistance at the y-intercept corresponds to the resistance of the two contact pads (6 Ω). These resistances were subtracted from the chain resistances and plotted by

the number of ETWI in the chain (Figure 5-17). The slope of the resulting line gives an average single ETWI resistance of 13 Ω.

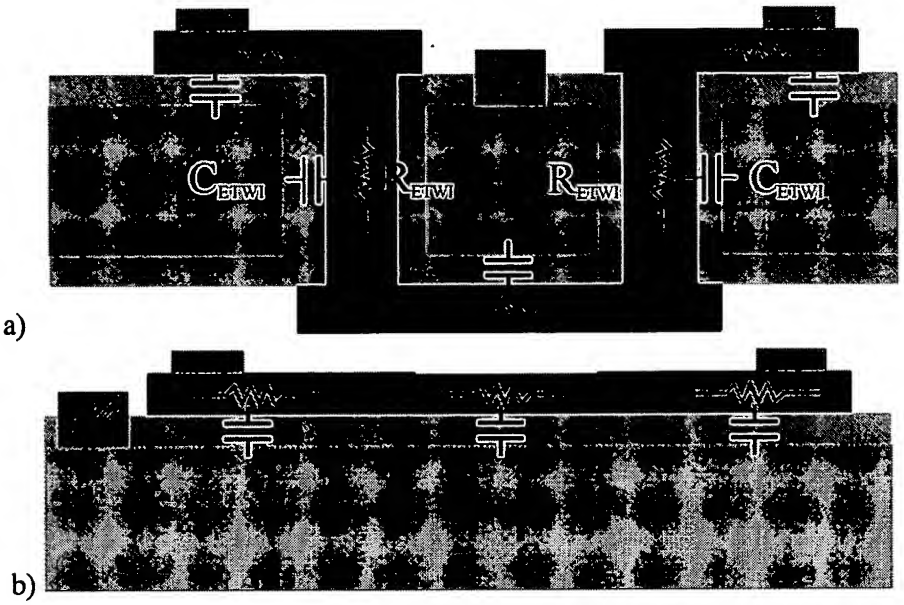


Figure 5-15. Schematic of ETWI chain geometery with resistance and capacitive contributions from a) ETWI chains and b) planar test structures.

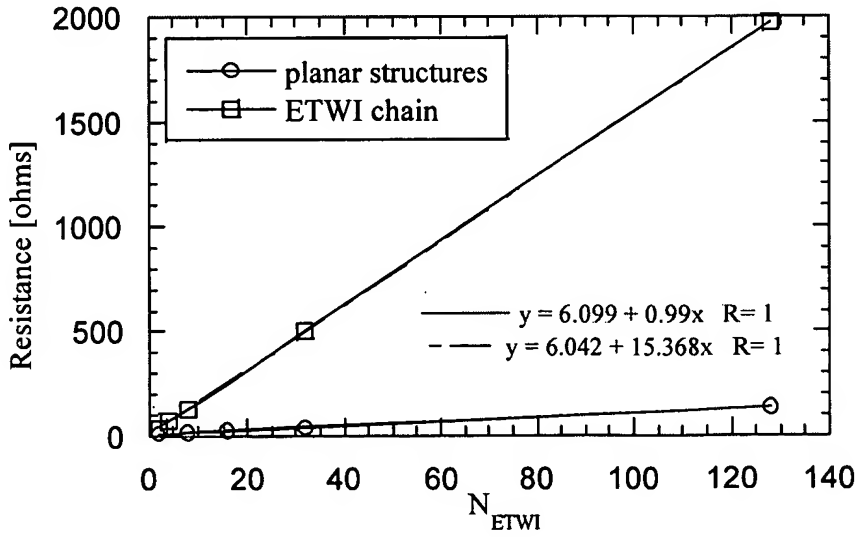


Figure 5-16. Resistance measurements of n-type ETWI chains and corresponding planar test structures. Measurements were made for N_{ETWI} = 2, 4, 8, 16, 32 and 128.

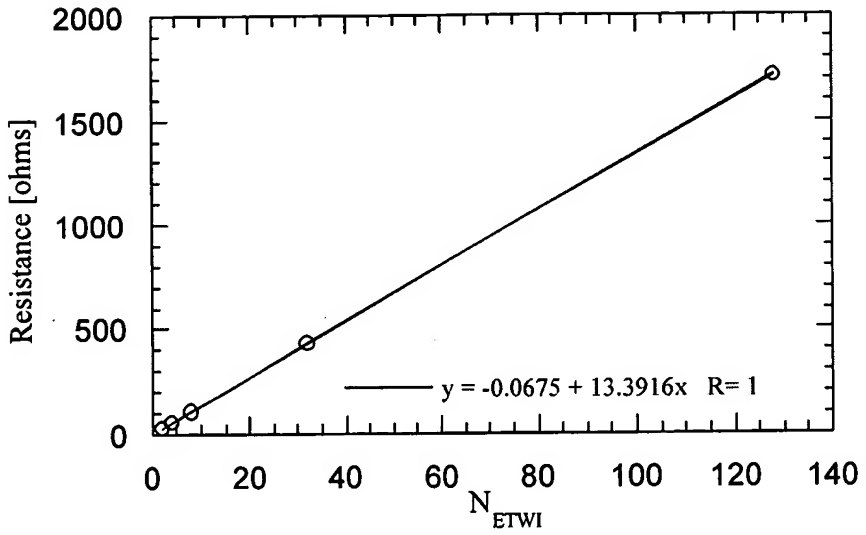


Figure 5-17. Resistance of n-type ETWI chains with the resistance of the connection lines and contact pads removed.

This extracted resistance is over two times greater than the theoretical minimum predicted in Section 5.1.1. Four point probe measurements were performed to obtain a doped polysilicon sheet resistance $R_s = \rho/t$ of 1.1 Ω/?, where t is the film thickness. This was not the theoretical minimum, suggesting that lower resistances could be obtained through increased doping and annealing. Using this measured resistivity and Equation 5-1 for $L = 415$ μm gives a resistance of 14 Ω, which corresponds with the extracted value above.

The resistance of p-type ETWI was similarly measured. A resistance of 24 Ω was measured for single ETWI that had undergone two doping cycles. For ETWI that had three doping cycles, 10 Ω was measured for each ETWI (Figure 5-18). Section 5.1.1 predicted 25 Ω per ETWI as the theoretical minimum for this geometry. If the radius of the ETWI is increased by three microns, the predicted minimum resistance is 12 Ω. This suggests that both doping and possible geometry discrepancies (due to mask erosion) from theory could explain the slight difference between the measured and predicted resistance.

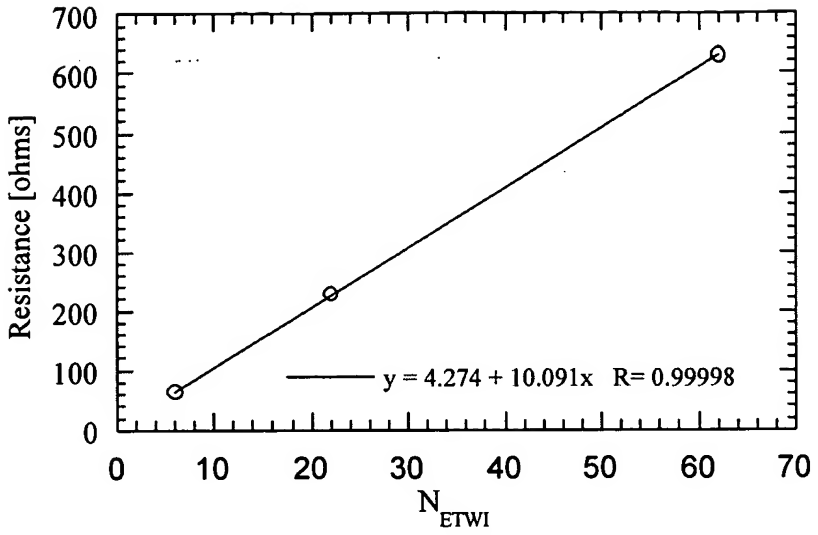


Figure 5-18. P-type chain resistance as a function of the number of ETWI.

The shield resistance measurements were complicated because specific test structures were not made for this measurement. Only one shield contact pad was fabricated for each ETWI chain, while two are needed for a resistance measurement. However, the shield was patterned and isolated for each ETWI. The backside of a wafer was processed to open contacts to the shield at the ends of the chain. This enabled measurement of a resistor network. Figure 5-19 shows the R_{shield} network for a chain with three ETWI.

The task was then to extract $R_{shield\text{-}via}$ from measurements of R_{12}, while also accounting for R_{leg} and R_{pad}. Planar test structures were used to measure R_{leg} at 2.8 $\Omega \pm 3$ ohms. This full network was measured for different N_{ETWI} to extract R_{pad} from the y-intercept, similar to the R_{ETWI} measurements. This network was not patterned as a meandering resistor chain as the R_{ETWI} chains were, and instead had many resistors in parallel. This made the R_{12} values very low and difficult to measure consistently. This was further complicated by the fact that aluminum pads were not available, and the n-type polysilicon had to be probed directly. Thus R_{pad} measurements were found to vary between 14 and 18 ohms.

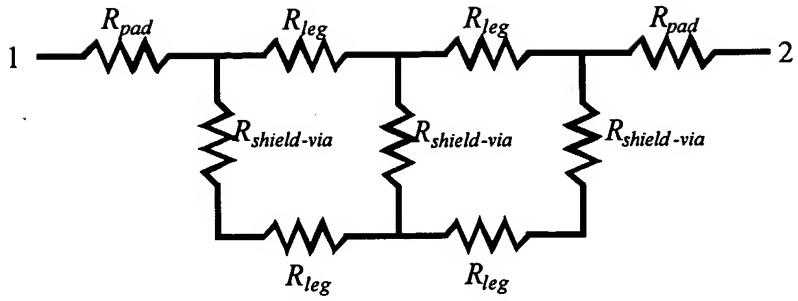


Figure 5-19. R_{shield} resistor network for ETWI chain of $N_{ETWI} = 3$.

To solve for $R_{shield\text{-}via}$, analytical and numerical techniques were used. The $N_{ETWI} = 2$ case can be solved analytically, but requires a very accurate R_{pad} measurement. The variation of 4 Ω in the R_{pad} value made the range of $R_{shield\text{-}via}$ several orders of magnitude, including non-physical values. For the N_{ETWI}= 128 case, the error in R_{pad} is less significant. A resistance of 208 ± 2 Ω was measured for R_{12} when $N_{ETWI} = 128$. A numerical circuit solver (HSPICE) was used to fit $R_{shield\text{-}via}$ to this value. An $R_{shield\text{-}via}$ of 10-100 Ω was obtained, with the large range due to the variability of R_{pad}. This range includes the predicted R_{shield} from Section 5.1.2 which was approximately 60 Ω.

It is important to note that even with an accurate $R_{shield\text{-}via}$ value, an estimate needs to be made for the effective R_{shield} to be used in a lumped circuit model of the chain. The shield contact was always placed in the center of the chain. This meant that ETWI in the middle of the chain had a shorter path to the ground pad than ETWI on the edges. A simple approximation is to take the average resistance seen from each ETWI to the ground shield. This means the effective R_{shield} varies with the length of the chain, and ranges from about 50 to 250 Ω. Fitting the shielding measurements is another way to estimate R_{shield}. Unfortunately, as detailed in Section 5.3.5, parasitics due to the measurement setup prevented an accurate value for the shielding, and thus a good estimate of R_{shield}.

Another consideration that affects the resistance measurements is the fact that the shield was partly oxidized during fabrication. This increases the resistance of the shield because oxidation consumes the polysilicon. However, phosphorus dopants segregate to

the polysilicon side of the oxide/polysilicon interface, meaning oxidation of heavily doped polysilicon can actually increase conductivity, albeit limited by the solid solubility limit [100].

5.3.3. Capacitance

Capacitance for a single ETWI was extracted from chain measurements, analogous to the resistance measurements. Capacitance as a function of bias voltage was measured across each oxide layer. Low frequency capacitance-voltage (LFCV) measurements using an HP4140B Picoampere Meter were used to obtain the maximum capacitance, which is the capacitance across the oxide when biased into accumulation. Because these substrates were not heavily doped (2×10^{14} cm^{-3} to $2\times10^{15}cm^{-3}$ of phosphorus), biasing into depletion adds a series capacitor which lowers the capacitance. The substrate is grounded and the conducting polysilicon layer voltage is swept, taking the capacitance through depletion, and then into accumulation, with a flat band voltage of $V_{sub\text{-}shield}$ = -2.7 V. The oxide capacitance (C_{ox}) is measured for both inversion and accumulation, as both conditions approximate a parallel plate capacitor. A typical LFCV curve is given Figure 5-20, with C_{ox} of about 52 pF.

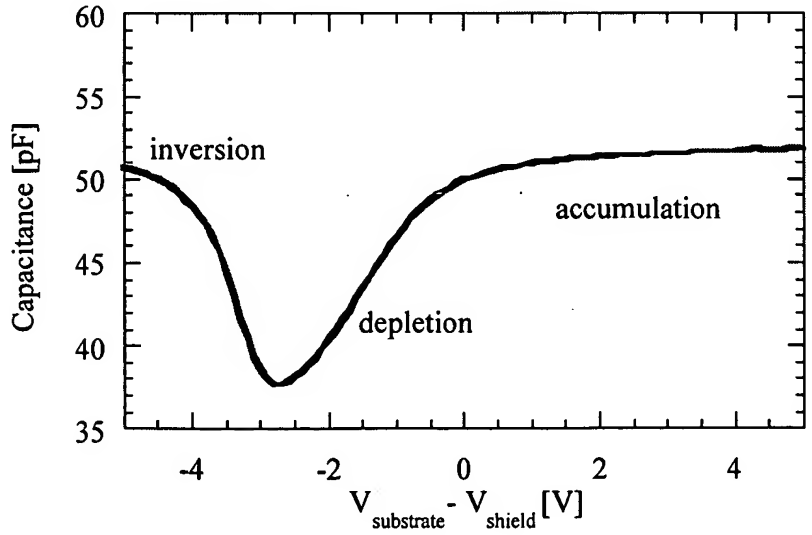


Figure 5-20. Low frequency capacitance-voltage (CV) measurement from the shield to the substrate for a shielded ETWI chain of length N_{ETWI} = 8.

High-frequency capacitance-voltage (HFCV) measurements were also performed. For measurements to the substrate, this provides a measure of the series resistance associated with the substrate or the substrate contact. When a series RC model is used for a high-frequency CV measurement, the real part of the impedance corresponds to the series resistance [101]. Standard open and short calibration of the capacitance associated with the probes and the coaxial cables was performed with an HP4275A LCR meter. Figure 5-21 depicts a high-frequency CV curve clearly showing the regions associated with accumulation and depletion. Typical of metal-oxide-semiconductor (MOS) HFCV curves, the inversion layer charge is not able to keep up with the modulation frequency of 10 KHz and C_{ox} is not observed in inversion. A series resistance (R_{sub}) of 300 kΩ is measured for an accumulation C_{ox} of 50 pF. Due to a fabrication processing error, the contact to the substrate was not heavily doped, so an ideal ohmic substrate contact was not expected. Thus this resistance is likely from the substrate contact, in addition to the substrate. R_{sub} was found to decrease by 10-25% when the frequency was increased to 100 kHz. For measurements of different devices with the same structures, R_{sub} varied from approximately 100 kΩ to 1 MΩ. R_{sub} also did not scale with the length of the chain, though the exact position of the substrate contact relative to the ETWI chain varied with the chain. The presence of R_{sub} has implications for the shielding measurements, and will be discussed in Section 5.3.5.

When HFCV or LFCV measurements are taken between the shield and the signal, no depletion region is observed (Figure 5-22). Both the shield and the signal are heavily doped polysilicon, so the measurement is akin to two parallel metal plates and the capacitance is constant.

The goal of measuring C_{ox} for a single ETWI was accomplished by recording C_{ox} from the LFCV curve of ETWI chains and their corresponding planar test structures. For an unshielded ETWI, the measured capacitance between the signal ETWI and the substrate is given in Figure 5-23. From this plot, Figure 5-24 is generated, resulting in ETWI capacitance only, as the capacitance due to the planar lines between the ETWI and the bond pads (1 pF) is removed. The slope of the fitted line results in a measured 0.6 pF per ETWI (Figure 5-24), which matches well with the predicted 0.5 pF of Section 5.1.1.

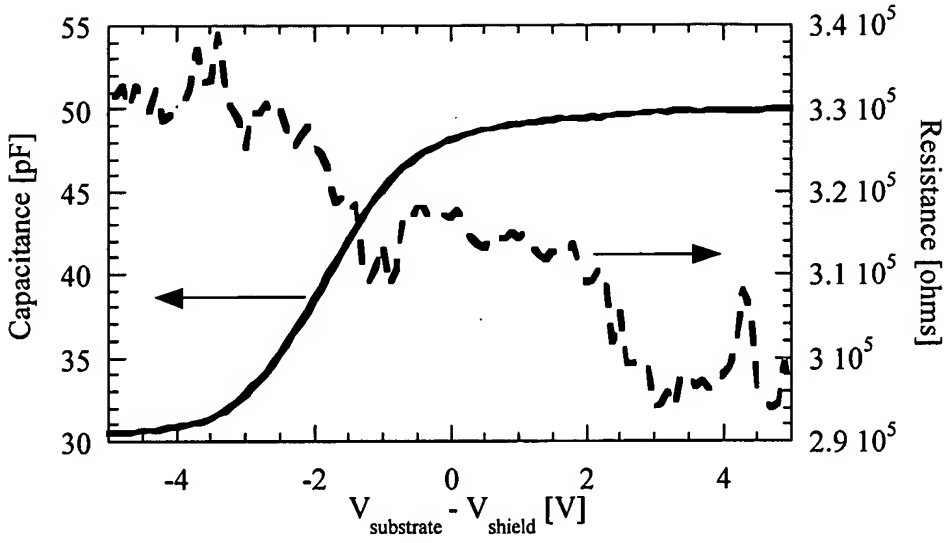


Figure 5-21. High-frequency CV curve taken at 10 KHz for C_{ox} across between the shield and substrate of a shielded ETWI chain (N_{ETWI} = 8). Extracted series resistance and the noise associated with the measurement is also shown.

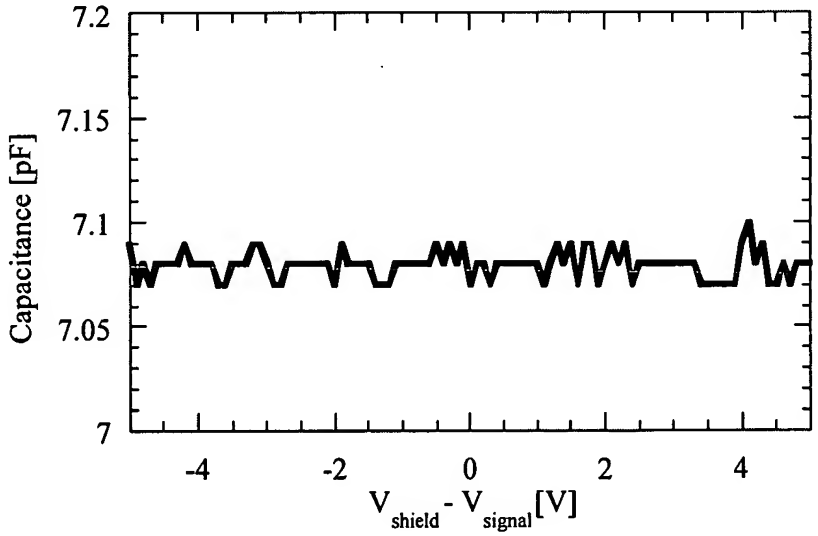


Figure 5-22. CV measurement between the shield and signal (both heavily doped). The quantization is due to the resolution limits of the current meter of the CV equipment.

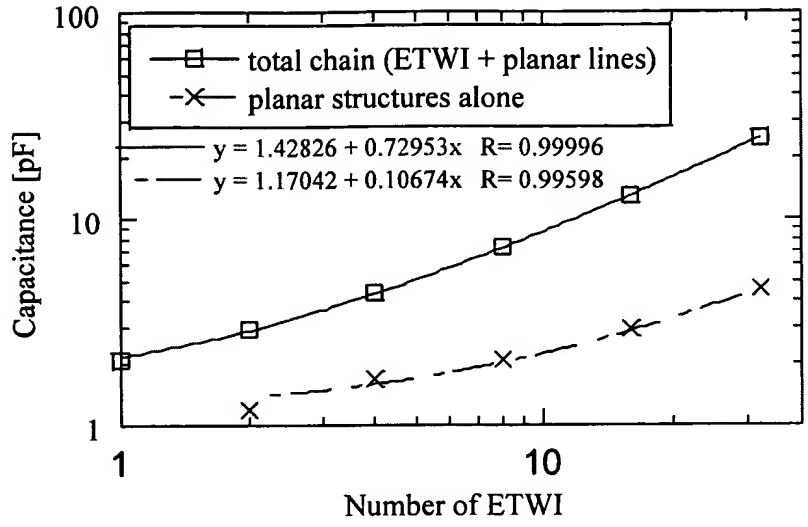


Figure 5-23. Capacitance measurements of ETWI chains and corresponding planar test structures.

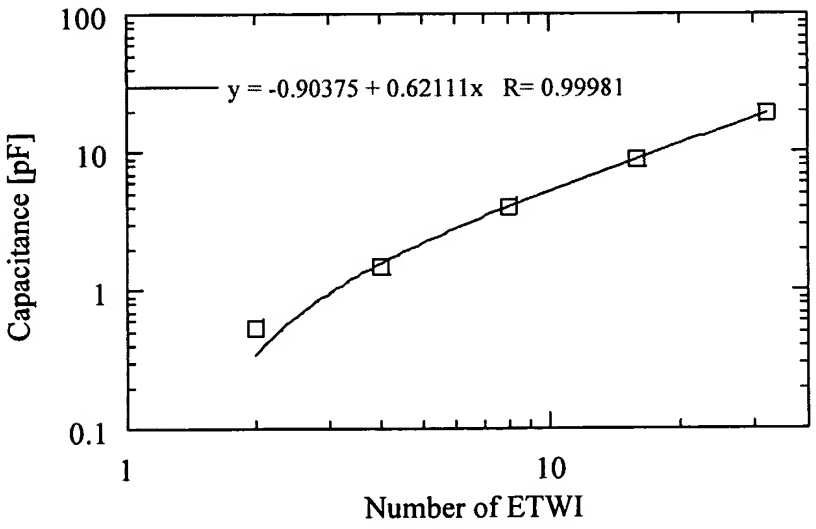


Figure 5-24. Capacitance of ETWI chains with the capacitance of the connection lines and contact pads removed.

For devices with shields, the oxide capacitance between the substrate and shield was similarly compiled. The difference between the curves in Figure 5-25 is plotted in Figure 5-26 to give an average oxide capacitance of 3.3 pF between the shield and the substrate. Section 5.1.2 predicted 1 pF for 1 μm oxide. The process logs indicate that 0.6

μm of thermal oxide was grown on the substrate prior to the shield deposition, instead of the intended 1 μm. Accounting for a slightly thicker substrate (415 μm instead of 400 μm) and varying the radius of the via because of mask erosion (10 μm to 13 μm) increases the capacitance prediction to 2 pF. Another source of the increased capacitance is the rough etch caused by the through-wafer etch (Figure 5-7). The thermal oxide grows at the silicon interface and consumes silicon at an oxide to silicon ratio of about 2 to 1. The roughness, on the order of one micron, would be smoothed after the long 2 μm oxidation performed for the non-shielded ETWI. However, for the shielded ETWI, only 0.6 μm was grown, so much of the roughness would remain and result in increased surface area, and thus increased measured capacitance.

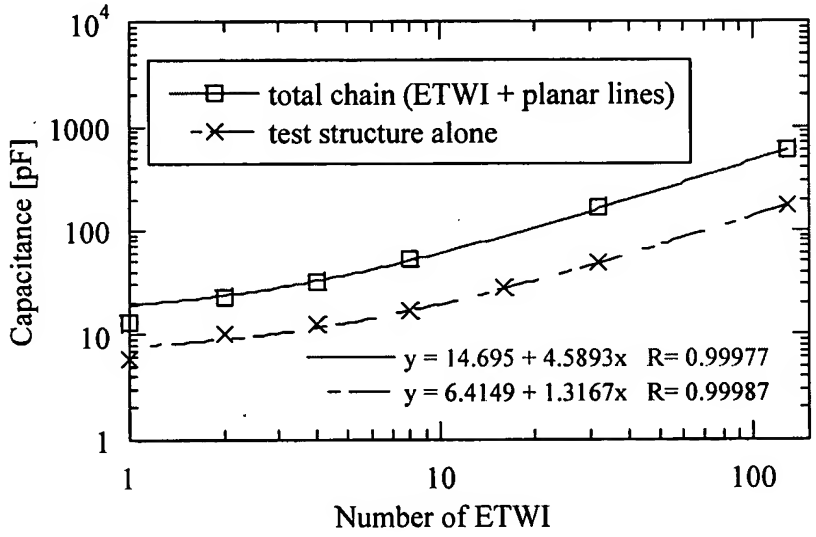


Figure 5-25. Oxide capacitance measurements between the shield and substrate for interconnect chains and their planar test structures.

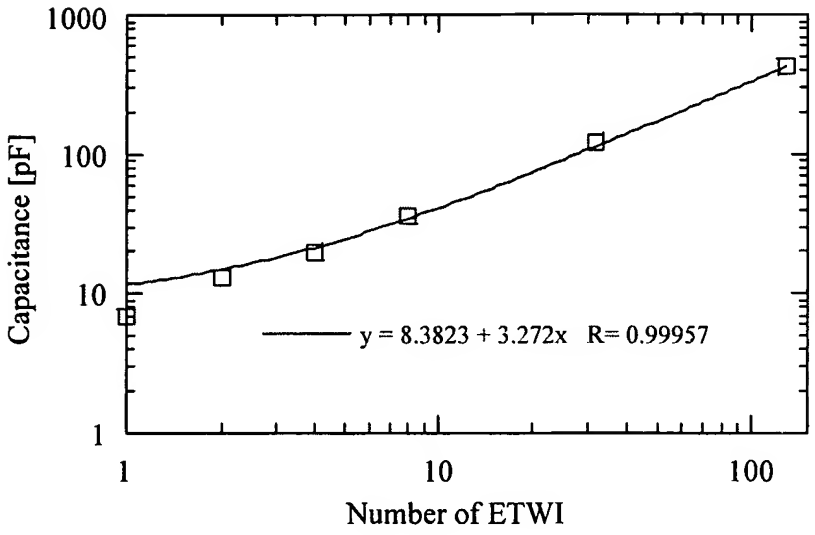


Figure 5-26. Extracted shield-substrate capacitance for the interconnect via only. The slope gives an average capacitance of 3.3 pF.

While the focus here was on measuring C_{ox}, CV curves are powerful tools for characterizing other important oxide qualities. Silicon/oxide or polysilicon/oxide interface charge can cause hysteresis or distortion in CV measurements and vary the threshold voltage of a MOS device from its designed value. This would have important implications for an ETWI connected to a device that measures charge or capacitance. The slight elongation of the transition from inversion to accumulation in Figure 5-20 and Figure 5-21 is generally characteristic of interface charge. A potential source of interface charge along the silicon through-wafer via is polymer from the etching process (see Section 2.1.4). Steps performed during the process to clean the vias included an oxygen plasma etch, a hydrofluoric acid etch, and a thermal oxidation. In addition, the process included a hydrogen anneal at 400°C to help hydrogen passivate dangling bonds associated with the interface [100]. However, this structure required diffusion through half of an entire wafer (200 μm, diffused from both sides), and the two hour hydrogen anneal used may not have been sufficient. To mitigate the effect of fixed oxide charges, high temperature argon anneals were performed (2 hours at 1000°C), but the effectiveness of this anneal also depended on diffusion through 200 μm of polysilicon, oxide, or silicon.

5.3.4. Leakage Current

The isolation across the oxide was measured with DC IV curves (Figure 5-27). The measurements were performed in a shielded box with nitrogen gas blowing on the surface to reduce surface leakage. The leakage was measured across a two micron thermal oxide separating the polysilicon signal ETWI and the polysilicon shield, and found to be less than 1 pA at 3 volts. The length of the chain did not significantly affect the measurement, as N_{ETWI} = 8 and N_{ETWI} = 32 both had currents of about 0.5 pA at 3 volts. The thinner oxide, 0.6 μm, between the etched silicon substrate and the polysilicon shield, was also measured. An increased leakage of 10 pA at 3 V was observed. This leakage did appear to scale with the length of the chain, as N_{ETWI}= 32 had about twice as much leakage. Higher leakage currents are expected across the shield because the oxide is thinner. Increased leakage currents have been reported for oxide on polysilicon, and are generally associated with the rougher surface of polysilicon versus silicon [94, 100], while long high-temperature oxidations (2 μm) which round out corners through oxide reflow are associated with reduced leakage [102].

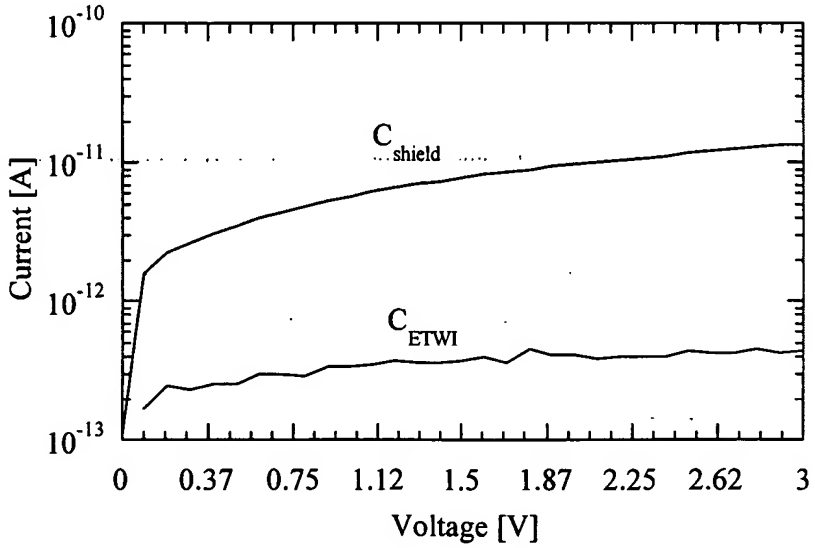


Figure 5-27. Measured DC leakage through 2 μm oxide between the signal ETWI and the shield (C_{ETWI} leakage) and through 0.6 μm oxide between the shield and the substrate (C_{shield} leakage) for ETWI chains of length N_{ETWI} = 8.

5.3.5. Shielding

To measure the effectiveness of the shielding, we applied a voltage to the substrate and measured the noise spectrum across the core signal ETWI. The measurement adds two parasitic components that are artifacts of the measurement technique: the substrate resistance and the probe capacitance. These were not taken into account when the shielding was predicted in Equation 5-5, so we describe here a model with these parasitic components. As previously described in the HFCV measurements above, a series resistance of 300 - 1000 kΩ was measured for the substrate contact. This was attributed to a processing error, where the substrate was not highly doped, which prevented the formation of an ohmic contact at the surface.

The capacitance between the probe on the substrate contact and the probe on the ETWI chain is also considered an artifact of the measurement process. The HFCV measurements were not subject to a parasitic probe capacitance because measurements were performed with an LCR meter that could remove this effect by calibration. For the shielding measurements, the probes were directly attached to a signal generator (connected to substrate probe) and the Wheatstone bridge noise measurement circuit (connected to signal ETWI), so automatic calibration was not possible.

To account for these artifacts of the measurement process, the effect of the probe capacitance was measured and accounted for in a lumped circuit model. To measure the coupling, the substrate probe was placed in air, a few millimeters above the substrate contact, but not in contact with the substrate. The other probes were placed on the ends of the ETWI chain to be measured and connected into the noise measurement circuit. One volt AC was applied to the suspended substrate probe and the signal coupled to the ETWI chain resistor was observed on the frequency analyzer. The measurement was repeated for different length ETWI chains, and for each frequency decade between 100 Hz and 100 kHz. The frequency spectrum of the ETWI signal and the substrate signal were measured in the same bandwidth and with the same resolution. The ratio of the measured peak values, a measure of the coupling due to the probes, is plotted in Figure 5-28.

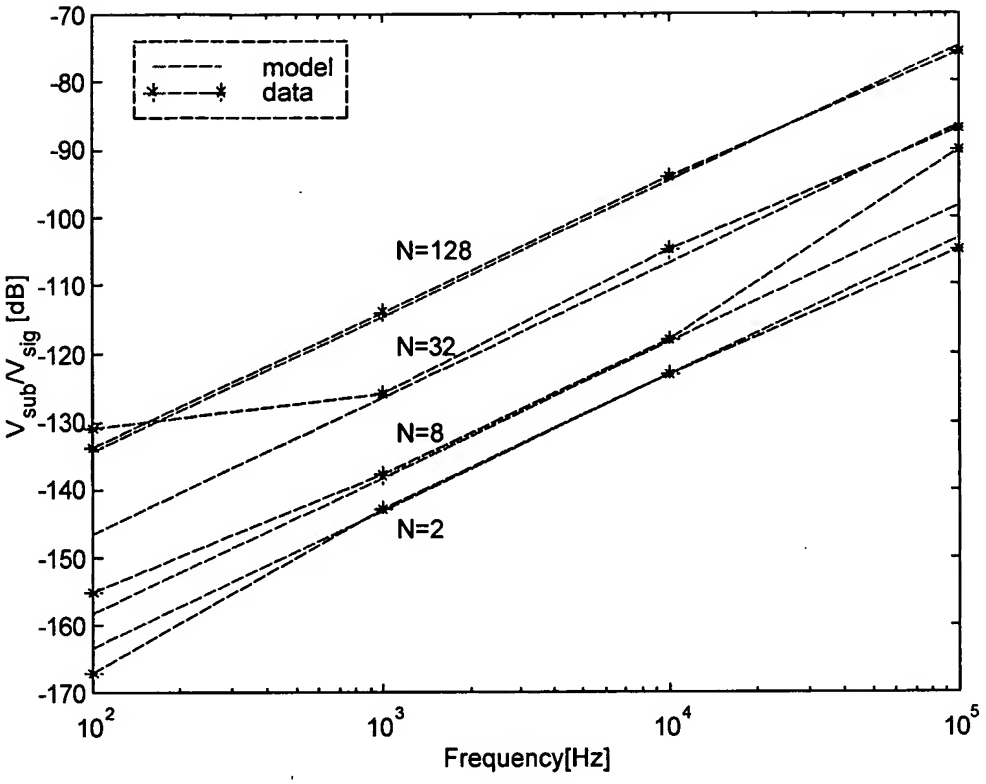


Figure 5-28. Probe capacitance measurement points and model for each ETWI chain.

The parasitic coupling due to the probe can be modeled as a series capacitor and resistor voltage divider. The capacitance is the fixed probe-probe capacitance, and the resistance is the ETWI chain resistance that varies from 30 - 2000 Ω, depending on the number of ETWI in the chain. The coupling is then

Equation 5-6 $$\frac{V_{sig}}{V_{sub}} = \frac{R_{etwi}}{Z_{C_{probe}} + R_{etwi}},$$

where V_{sig} is the ETWI signal, V_{sub} the suspended substrate signal, R_{ETWI} the ETWI chain resistance, and Z_{Cprobe} the impedance of the probe-to-probe capacitance C_{probe}. This model was fitted to the data in Figure 5-28 with a C_{probe} value of 0.3 pF.

The lumped RC model for the ETWI shielding measurement now needs to include two components which do not scale with the number of ETWI: R_{sub}, the substrate

resistance, and C_{probe}, the probe-to-probe capacitance. All of the components of this model have been experimentally measured (Figure 5-29).

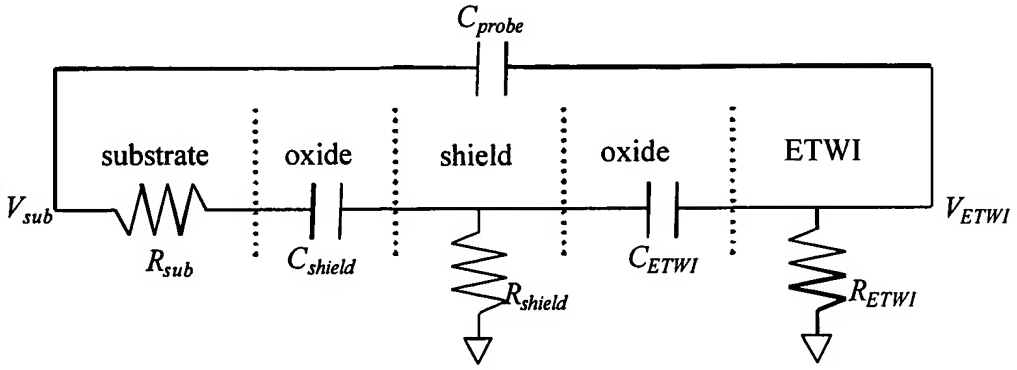


Figure 5-29. Lumped RC model of shield with measurement parasitics.

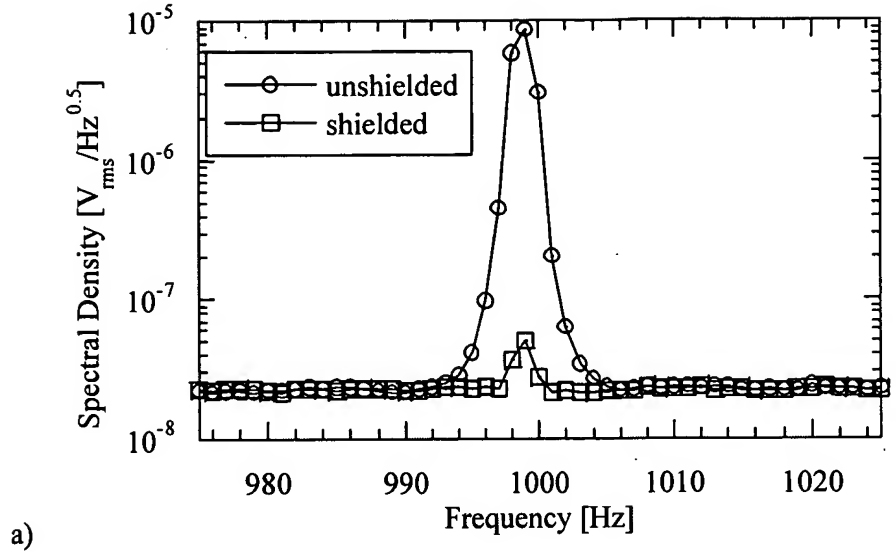
The coupling between V_{ETWI} and V_{sub}, now altered from Equation 5-5, and is now given by

Equation 5-7 $$\frac{V_{etwi}}{V_{sub}} = Z_1 Z_2 + Z_3,$$

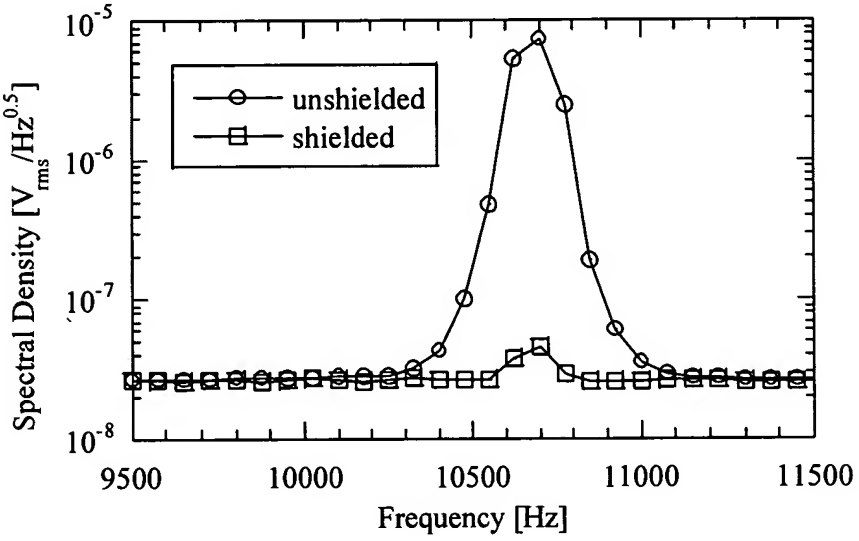
where $Z_3 = \frac{Z_{device}}{Z_{C_{probe}} + Z_{device}}$ and $Z_{device} = \frac{1}{2} R_{etwi} \| \left(Z_{C_{etwi}} + R_{shield} \| Z_{C_{sub}} \right)$.

Terms Z_1 and Z_2 were defined in Equation 5-5. Term Z_3 includes the effect of the parasitic probe capacitance. This term approaches zero as the probe capacitance goes to zero.

To measure the effectiveness of the ground shield, the substrate was driven with the probe in contact with the pad. The noise spectrum of the ETWI was measured using the Wheatstone bridge circuit described above, similar to the probe capacitance measurement. Figure 5-30 shows how the substrate signal coupling to the ETWI is suppressed by over two orders of magnitude at 1 kHz and 10 kHz when the shield is driven by a ground signal, relative to when the shield is unconnected.



a)



b)

Figure 5-30. ETWI signal when substrate is driven by 25 mV signals. Shielding reduces the coupling to the ETWI by over 2 orders of magnitude for a) 1 kHz and b) 10 kHz substrate signals.

The effectiveness of the shield as a function of frequency was measured by varying the frequency of the applied substrate signal. Measurements similar to Figure 5-30 were repeated for each frequency decade between 100 Hz and 100kHz. Higher frequencies were beyond the bandwidth of the amplifier. The ratio of the shielded and unshielded peak signal in the noise spectrum is plotted as a function of frequency for a

chain of length N_{ETWI} = 128 in Figure 5-31. Approximately 50 decibels of shielding are observed over this frequency range.

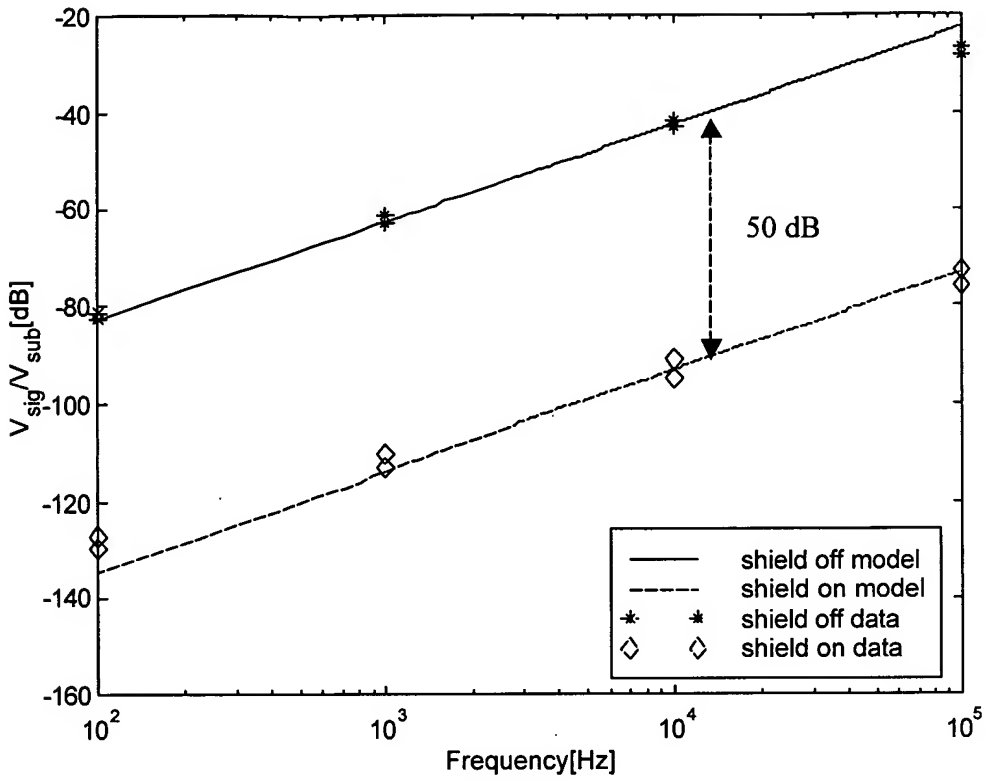


Figure 5-31. Absolute magnitude of shielding as a function of frequency for ETWI chain of length N_{ETWI} = 128. The measured data points at each decade are plotted, along with a lumped circuit model.

The model of the N_{ETWI} = 128 ETWI, given in Equation 5-7, is also plotted in Figure 5-31, using the measured component values R_{ETWI} = 2 kΩ, C_{ETWI} = 120 pF, R_{shield} = 100 Ω, C_{shield} = 600 pF, R_{sub} = 300 kΩ, and C_{probe} = 0.3 pF. For the unshielded case, R_{shield} is set to infinity. To see the effect of the parasitics, it is useful to compare the components of the model, Z_1*Z_2 and Z_3, which were defined in Equation 5-7. For the N_{ETWI} = 128 case, term Z_3, which represents the effect of the probe capacitance, is negligible in the unshieled case, but significant in the shielded case (Figure 5-32). For the N_{ETWI} = 2 case, we use the N_{ETWI} = 2 measured components and see that the probe capacitance term Z_3 still does not affect the unshielded case, but now dominates the

shielded case by a few orders of magnitude (Figure 5-33). The slight change in slope observed in the shielded model for N_{ETWI} = 128 below 1 kHz, and N_{ETWI} = 2 below 30 kHz, is due to the substrate series resistance. However, this effect is overwhelmed by the probe capacitance term.

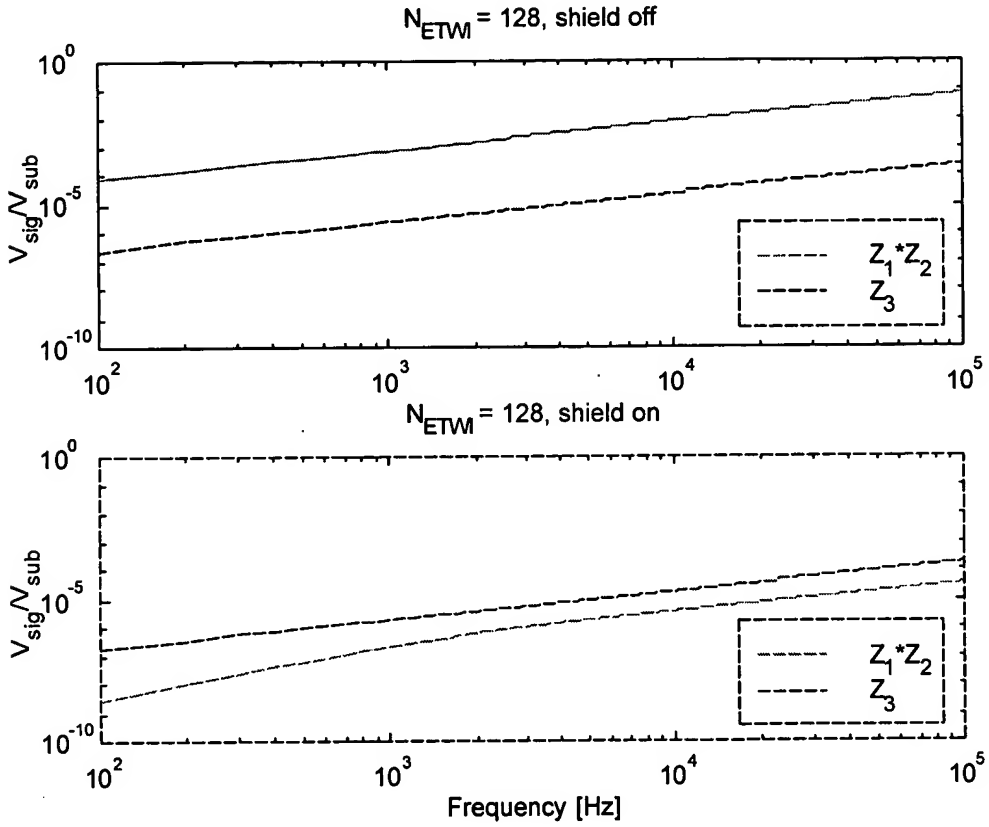


Figure 5-32. Absolute magnitude of N_{ETWI} = 128 model components for shielded and unshielded ETWI.

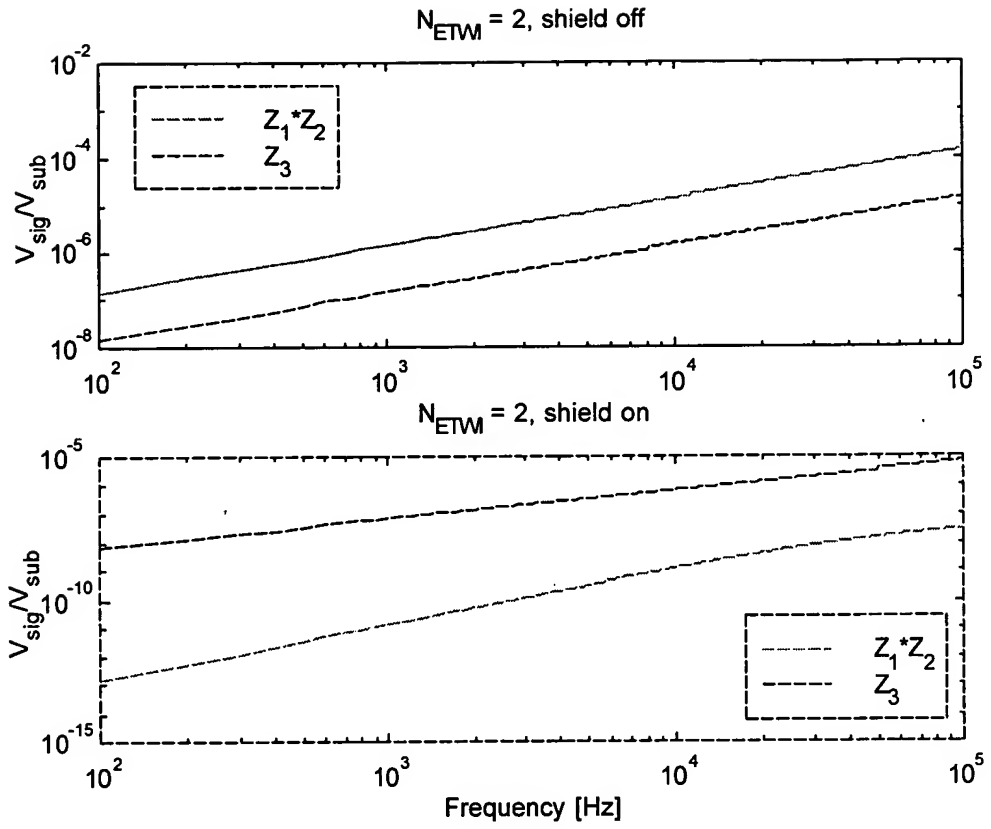


Figure 5-33. Absolute magnitude of $N_{ETWI} = 2$ model components for shielded and unshielded ETWI.

The measured difference between the coupling for a shielded ETWI and the coupling for an unshielded ETWI can be referred to as the relative shielding. Because the probe parasitic does not scale with the number of ETWI and is larger than the coupling through the ETWI shield, the measured relative shielding appears to decrease as the ETWI chain length decreases. Figure 5-34 shows the relative shielding decreasing from 50 dB for $N_{ETWI} = 128$ to less than 30 dB for $N_{ETWI} = 2$. Because the probe capacitance dominates the measurement, we are not able to measure ETWI shielding alone and cannot extrapolate to compare with the predicted relative shielding of 100 dB for one ETWI at 100 kHz (Section 5.1.2). Table 5-1 summarizes the shielding models and measurements.

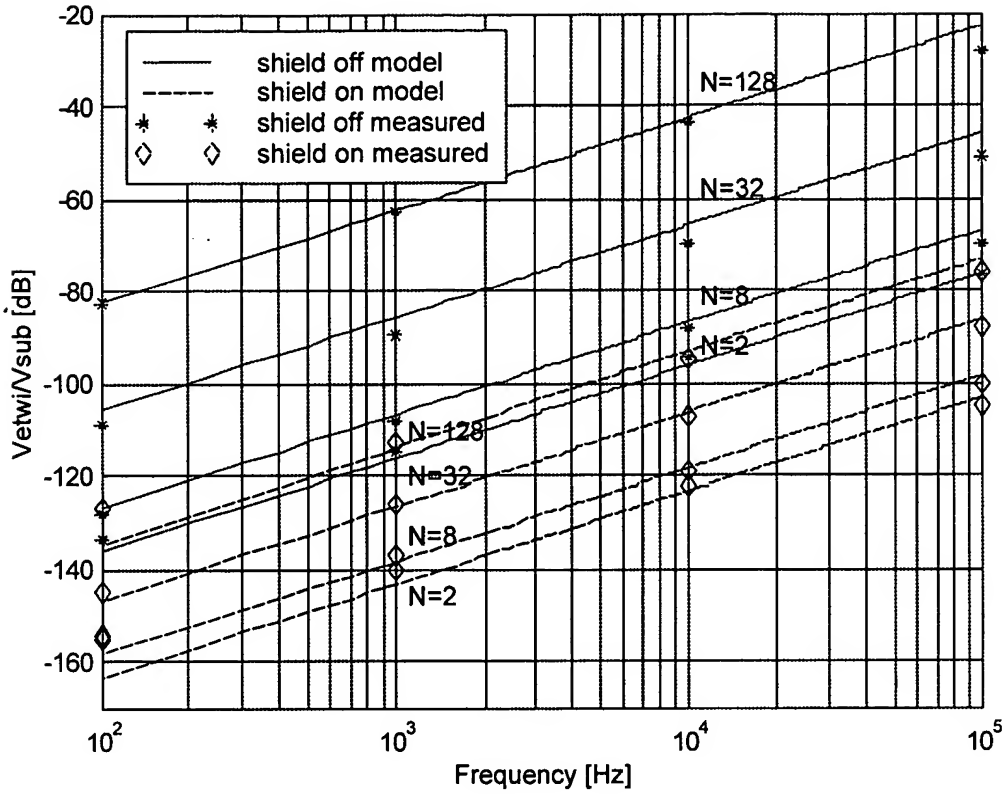


Figure 5-34. Measured and modeled substrate to ETWI coupling (absolute magnitude) for various length ETWI chains.

	ETWI alone - model			ETWI with parasitics - model			Measured	
ETWI chain length	Component values (Figure 5-3b)	Predicted shielding: $V_{ETWI}/V_{substrate}$ [dB] at 1 kHz		Component values (Figure 5-29)	Predicted shielding: $V_{ETWI}/V_{substrate}$ [dB] at 1 kHz		With parasitics: $V_{ETWI}/V_{substrate}$ [dB] at 1 kHz	
	R[Ω] C[pF]	Shield on	Shield off	R[Ω] C[pF]	Shield on	Shield off	Shield on	Shield off
$N_{ETWI}=1$	$R_{ETWI}=5$ $C_{ETWI}=0.5$ $R_{shield}=100$ $C_{shield}=1$	-270	-145	NA	NA		NA	
$N_{ETWI}=2$ . . .	$R_{ETWI}=37$ $C_{ETWI}=2.9$ $R_{shield}=100$ $C_{shield}=24$	-220	-115	$R_{ETWI}=37$ $C_{ETWI}=2.9$ $R_{shield}=100$ $C_{shield}=24$ $R_{sub}=200$ k $C_{probe}=0.3$	-143	-116	-140	-115
$N_{ETWI}=128$	$R_{ETWI}=1.9$ k $C_{ETWI}=121$ $R_{shield}=100$ $C_{shield}=620$	-130	-62	$R_{ETWI}=1.9$ k $C_{ETWI}=121$ $R_{shield}=100$ $C_{shield}=620$ $R_{sub}=200$ k $C_{probe}=0.3$	-115	-62	-116	-62

Table 5-1. Summary of shielding models and the predicted and measured shielding. The ETWI chains (N_{ETWI} = 2 and N_{ETWI}=128) include the effect of the connections between the ETWI. The parasitic effects of the substrate resistance and probe capacitance were added to the model and found to match the measured data.

5.3.6. Noise

Noise characteristics were measured by placing the ETWI chain in a matched Wheatstone bridge, in the same circuit used for the piezoresistive cantilevers and ETWI of the previous chapter. Devices were wire-bonded into hybrid IC packages to allow complete encapsulation of the device, with exterior shielding to protect from environmental noise (Figure 5-35). A chain of 128 n-type ETWI was compared to a metal film resistor, both with a resistance of 2000 Ω (Figure 5-36). The ETWI chain and

the reference resistor have nearly coincident noise curves, with similar low frequency and plateau characteristics. The 1/f noise at 10 Hz is 50 $nV/\sqrt{Hz}$, which agrees with previously reported results for heavily n-type doped polysilicon resistors [99]. Both measured noise spectra are limited by the system noise floor of 20 $nV/\sqrt{Hz}$ (described in Section 4.3.2) which exceeds the Johnson noise of a 2000 Ω resistor (5 $nV/\sqrt{Hz}$). P-type ETWI noise curves were also measured to be the same as a metal film reference resistor (Figure 5-37).

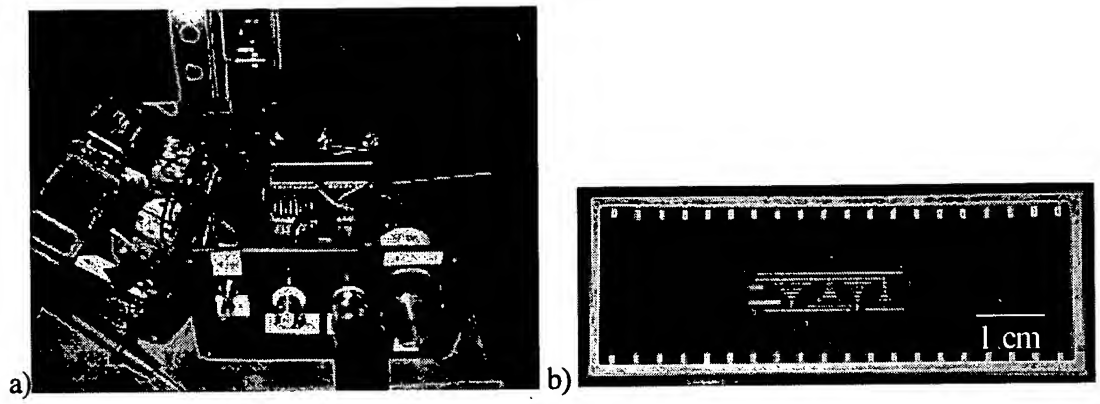


Figure 5-35. Image of a) test electronics and b) a packaged ETWI test chip.

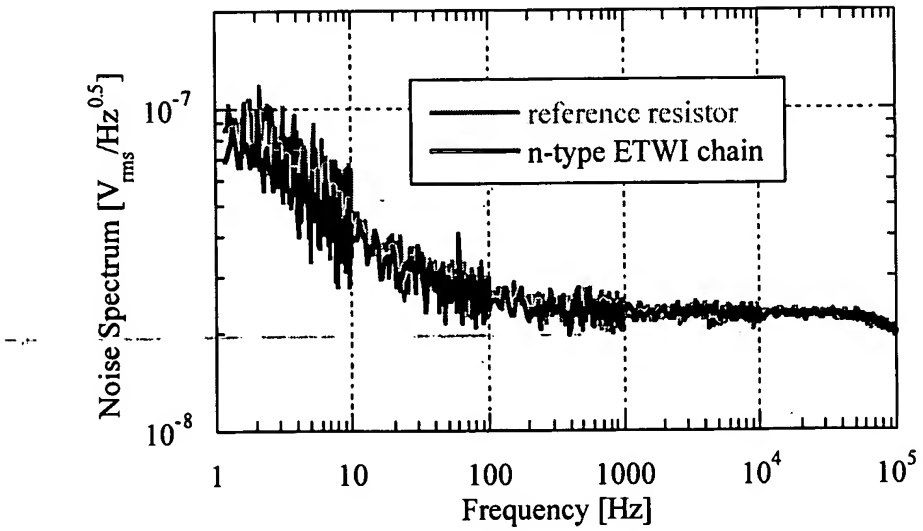


Figure 5-36. N-type ETWI noise spectrum for a chain with N_{ETWI} = 128 and and resistance of 2 kΩ.

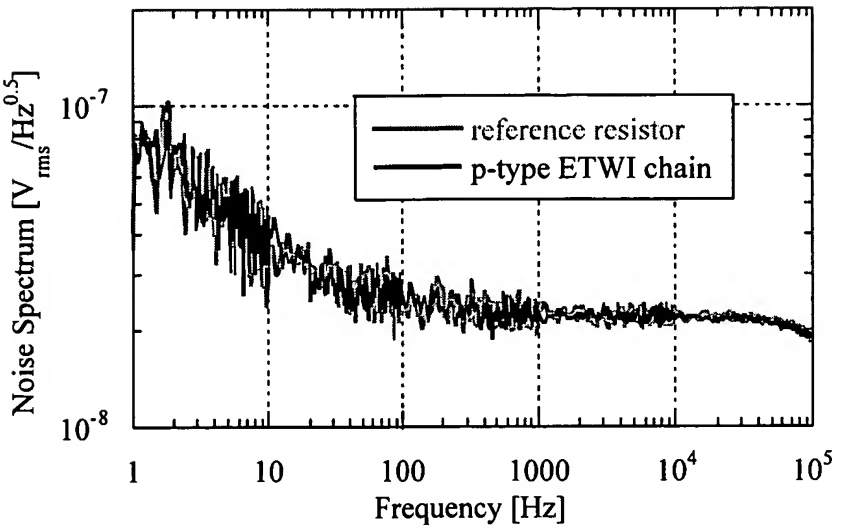


Figure 5-37. P-type ETWI noise spectrum for a chain with N_{ETWI} = 184 and 1 kΩ.

We are not able to measure the noise for a single ETWI because of the limits of the system electronics. Specifically, the noise due to the amplifier and the balance resistors in the bridge appear to be as noisy as the ETWI resistors. For a conservative calculation, we can assume our measured noise for a chain of 128 interconnects is at the measurement system noise floor. While the physical sources of flicker noise are an area of active research, an empirical relation has been shown to accurately describe flicker noise in many materials, including doped polysilicon resistors [98, 99]. This Hooge relation characterizes the power spectral density of voltage fluctuations as

Equation 5-8 $$S_v = \frac{\alpha V^2}{f^\gamma N},$$

where α is a dimensionless number characteristic of the material, V is the average voltage across the resistor, f the frequency, γ a constant typically between 0.7–1.3, and N the total number of carriers contained within the sample [88]. For a series of n ETWI, V voltage across the chain, and V_1 the voltage across one ETWI, $V = n\ V_1$. Similarly, for a total number of carriers in the chain N, and N_1 carriers in one ETWI, $N = n\ N_1$. Assuming all ETWI in the chain are identical then, the noise should then scale with the number of ETWI, and

Equation 5-9 $S_{v_n} = nS_{v_1}$,

where S_{vn} is the noise of the chain, and S_{v1} the noise of one ETWI. This suggests that the noise power of one ETWI is at least 128 times less then the chain of ETWI measured in Figure 5-36, and the measurements suggest that a single ETWI connected to a sensor would not increase the overall noise.

5.4. Conclusion

Through-wafer electrical interconnects which can be integrated with standard semiconductor processing have been demonstrated. Their small size (20 μm diameter) makes these devices attractive for high-density applications. Unlike previous work, the ETWI are filled and use high-temperature compatible materials, making them compatible with standard vacuum handling equipment and subsequent integrated circuit processing. The resistance of a single ETWI (14 Ω for n-type, 10 Ω for p-type) is adequate for piezoresistive applications, where the series sensor resistor is typically more than 1 kΩ. The low capacitance (less than 1pF) is attractive for capacitive sensors such as ultrasound transducer arrays. An integrated polysilicon shield was shown to reduce substrate coupling by 50 dB at 10 kHz for a 128 ETWI chain, as predicted by a lumped circuit model. Shielding measurements of shorter chains of ETWI were complicated by the existence of poor substrate contacts and excessive probe capacitance. Shielding reductions of 100 dB are predicted for single ETWI.

Chapter 6: Current and Future Work

The pre-processed polysilicon ETWI described in the previous chapter are currently being integrated into two types of ultrasound transducer arrays. One of the device arrays, based on a membrane capacitor, demonstrates the powerful way ETWI can be used to integrated separately optimized MEMS and IC processes. Work addressing the planarization of the ETWI will also be presented. Future prospects for pre-processed ETWI are then discussed. Materials issues are reviewed and suggestions made for future work. Finally, the challenge of integrating pre-processed ETWI into a manufacturing environment is addressed.

6.1. Current Work

Work is underway to integrate polysilicon filled ETWI with two different silicon micromachined ultrasound sensor arrays. The pre-process approach simplifies integration, as described in Section 1.3.3, because like cantilevers, the sensors are released devices which are difficult to process after being fabricated. The ETWI solve density and geometrical issues associated with electrically addressing arrays of sensors, similar to the cantilever array application described in Chapter 4. Both sensors have applications in water, so the packaging is greatly simplified when the wire-bonds are removed from the sensor side of the device.

6.1.1. Piezoresistive Membrane Sensor

The piezoresistive ultrasound proximity sensor project is a collaboration led by Venkataraman Chandrasekaran and Professor Mark Sheplak from the University of Florida. The devices are being fabricated at Stanford and use the p-type version of the polysilicon filled ETWI, without ground shields. The p-type ETWI data presented in Chapter 5 came from test runs for this project.

The device is a silicon membrane resonator and sensor that is designed to measure gas and liquid boundaries a few millimeters away. A membrane is driven with an embedded heater to thermally expand and generate ultrasound waves at a resonant frequency of 50 kHz. Piezoresistive deflection sensors are used to measure the reflected waves from the gas/liquid boundary. The process uses the anisotropic through-wafer plasma etching release techniques described in Chapter 3 to release the membranes. Just as for the piezoresistive cantilevers, accuracy in controlling the release is important for maximizing the sensitivity of the piezoresistive deflection sensors. The piezoresistors use p-type dopants, making a p-type ETWI preferable because it is simpler than n-type ETWI to integrate with p-type sensors. The experimentally measured resistance and noise characteristics reported in Chapter 5 are sufficient for integration with these sensors. A schematic of the device is given in Figure 6-1 and optical images of completed devices are given in Figure 6-2. Testing of the sensors and the ETWI is in progress [103].

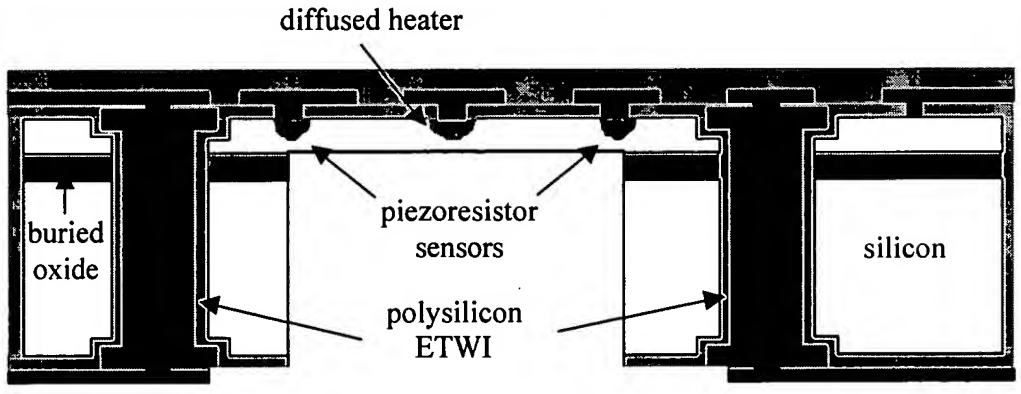


Figure 6-1. Schematic cross-section of a piezoresistive membrane sensor with integrated ETWI. Drawing courtesy of Venkataraman Chandrasekaran.

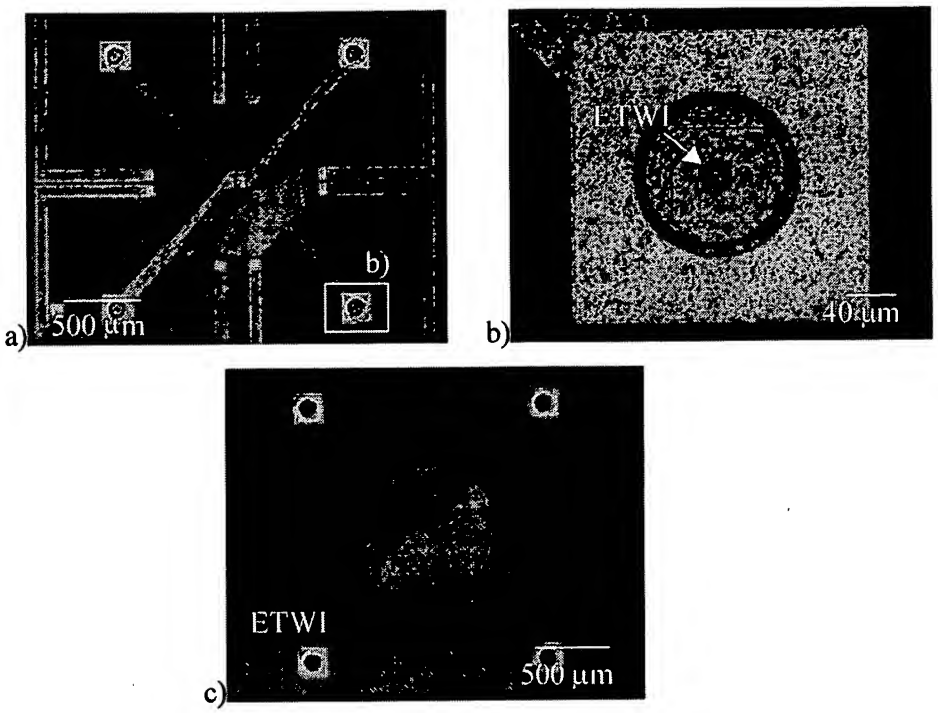


Figure 6-2. Images of completed piezoresistive ultrasound sensors with integrated polysilicon ETWI. a) Top-side view, with the membrane deflected. b) Close up of the ETWI. c) Backside view, looking at the membrane through the backside hole. Images courtesy of Venkataraman Chandrasekaran.

6.1.2. Capacitive Transducer

Capacitive micromachined ultrasonic transducers (CMUTs) are-released silicon sensors for applications in air-coupled nondestructive evaluation and liquid immersion imaging. Standard semiconductor processing is used to fabricate a parallel plate capacitor between two electrodes with a gap defined by a sacrificial thin film. This permits ultrasonic sensing in the megahertz range which is comparable to piezoelectric technology, with the advantage that the fabrication process is compatible with electronics integration [8, 47].

Two-dimensional arrays of CMUTs permit 3D imaging but require a means to electrically address individual elements with minimal area on the sensor side of the device. Integrated ETWI solve this problem, in addition to simplifying packaging for immersion applications. ETWI that are fabricated before the CMUTs are preferred as the CMUTs are released devices. At Stanford, under Professor Butrus Khuri-Yakub, researchers are fabricating 2D CMUT arrays with electronics, using integrated

polysilicon ETWI. A flip-chip approach is used to bring separate optimized sensor and circuit processes together into a highly integrated device, demonstrating the power of ETWI to help integrate MEMS and ICs (see Figure 6-3 and Section 1.2.3).

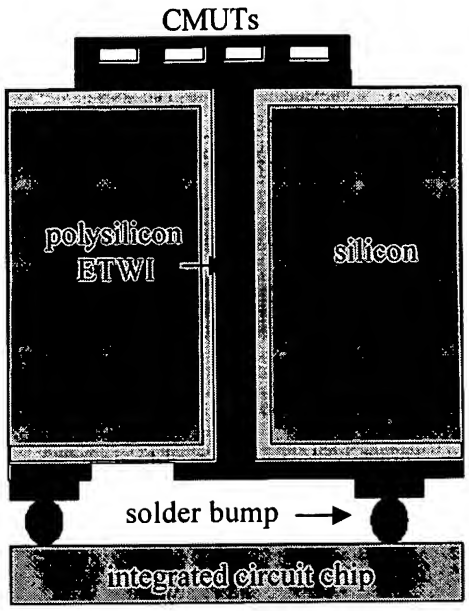


Figure 6-3. Capacitive ultrasound transducer connected to a signal processing IC with a polysilicon interconnect.

In this application the ETWI are in series with a capacitive sensor operating at high frequency, so lowering the capacitance of the ETWI is critical for maximizing sensitivity. Chapter 5 reported the capacitance of the pre-processed polysilicon filled ETWI alone as being less than 1pF. However, when integrated with this particular device, the parasitic capacitance of the ETWI pads on the top and bottom of the wafer becomes dominant. Figure 6-4 shows a patterned electrical connection to an ETWI. Ching-Hsiang Cheng and co-workers are working to lower the capacitance of both the polysilicon ETWI and the interconnect pads by integrating reversed bias junctions and using highly resistive substrate wafers [47].

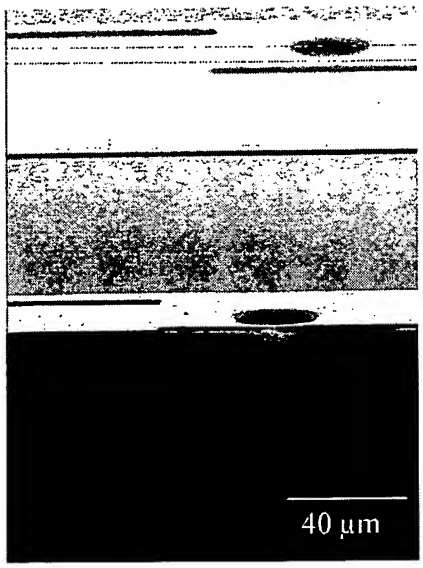


Figure 6-4. Cross section SEM of a patterned ETWI for integration with a CMUT array. Image courtesy of Ching-Hsiang Cheng.

6.1.3. ETWI Planarization

A pre-processed ETWI should be planar enough that it does not complicate fabrication of subsequent devices. For sensor processes which only need thick photoresist (more than 10 µm), the 3-5 µm dimple that forms in the ends of the ETWI is tolerable (see Figure 5.8c). When a smoother surface is required, plasma etch-back techniques can be used to remove the surface polysilicon while leaving smooth device layer films, including the electrical connection to the ETWI. In this approach the ETWI process of Chapter 5 was modified to include an oxide etch-stop layer after the first two microns of the ETWI polysilicon were deposited and diffusion doped (Figure 6-5a). To fully remove the roughness, however, chemical and mechanical polishing techniques standard to semiconductor manufacturing can be used. Polysilicon and oxide are thin films that are routinely planarized in the semiconductor industry to facilitate subsequent high-resolution lithography steps that require thin photoresist, and thus flat surfaces. In addition to using combinations of chemical and mechanical polishing, many IC processes use spin-on liquid films with the same etch rate as the polysilicon as a sacrificial layer for etch back planarization. Figure 6-5b demonstrates how a simple mechanical polish that was not semiconductor grade can be used to achieve less than one micron of roughness.

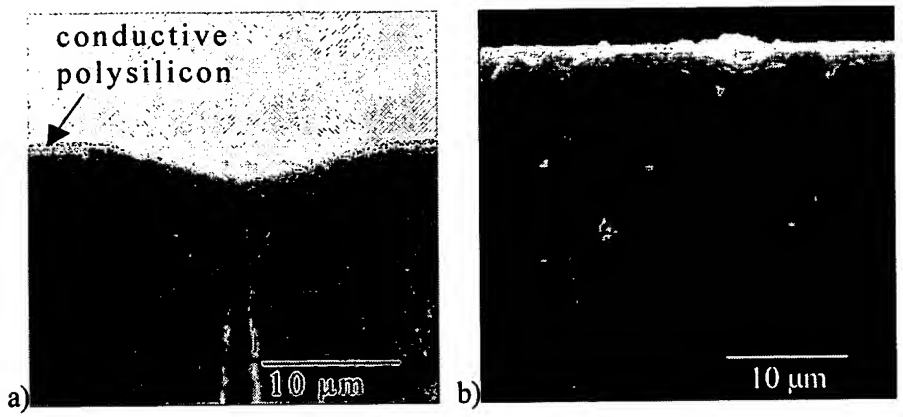


Figure 6-5. SEM cross section image of a polysilicon filled ETWI after planarization using a) plasma etch back (image courtesy of Ching-Hsiang Cheng) or b) mechanical polishing.

6.2. *Future Challenges for Pre-Process ETWIs*

The previous section and the discussions in Chapter 1 demonstrate the utility of a high-temperature compatible ETWI. An unfilled ETWI using tungsten as the conductor was demonstrated in this work, but this technology was shown to complicate future lithography. Hence the polysilicon filled approach is the technology currently being used for the two sensor arrays previously described. However, there is room to improve upon the polysilicon filled approach for making high-temperature compatible ETWI by investigating new process technologies and materials. After discussing new fabrication technologies, issues concerning integration and manufacturability of pre-processed ETWI will be addressed.

6.2.1. Fabrication Technology

The fabrication of pre-process ETWI requires three main steps: silicon etching, dielectric deposition, and then conductor deposition and filling. The device performance achievable will depend on how well optimized the fabrication process is for the particular geometrical and electrical requirements required for the application. The design of the filled ETWI done for this work (Section 5.1) introduced these issues, and demonstrated how materials processing limitations restricted the achievable design space.

Silicon through-wafer etching using TMICP techniques was shown in this work (Chapter 5) to be limited to an aspect ratio of 20:1 for a 400 μm thick wafer. Increasing this ratio would permit further reductions in footprint area and capacitance. As described in Section 2.5, TMICP etching has many variables which researchers are optimizing to increase etch rates, but it is not clear whether these approaches are achieving increased aspect ratios for circles [68, 69]. Recall that ETWI fabrication requires the etching of circles that are much more difficult to etch deep than the trenches used by most etching studies. Recently reported experiments and theoretical work are addressing the issue of ultimate aspect ratio, suggesting that consumption of species along the sidewalls is limiting reactant transport to the base of the vias where etching occurs [104, 105]. Hopefully advances in plasma hardware and new etch recipes will help to address this problem and enable higher aspect ratio through-wafer silicon etching.

The desired improvements in dielectrics for pre-processed ETWI depend on the application. For applications where the ETWI are used as wires and minimal impedance is required, reducing the achievable capacitance of the dielectric is the goal. This means increasing the thickness of the layer or reducing the dielectric permittivity. Thermally grown oxide, used in this work, is growth limited to a thickness of about two microns. Oxide can also be deposited, but the conformality is not sufficient for filled ETWI applications. We have done preliminary experiments which suggest that a super thick oxide (greater than 2 μm) can be grown by using sacrificial polysilicon layers. After growing two-microns of thermal oxide, we deposited polysilicon, which was then completely consumed by a subsequent thermal oxidation. This resulted in a thermal oxide with a thickness of 3.8 μm. Potentially this technique could be used to reduce the achievable capacitance of an ETWI. However, the stress of thick thermally grown oxide could complicate future processing. In addition, oxides grown on polysilicon can be of lower quality, meaning increased leakage currents and lower breakdown voltages. Currently the integrated circuit industry is developing low dielectric permittivity materials to reduce capacitive coupling between multiple layers of metal lines. Fluorine and carbon doped oxides, with a dielectric permittivity of 10-50% lower than thermal oxide, are potentially conformal and high-temperature compatible and thus worth investigating for low capacitance ETWI applications.

Integrated bypass capacitors are a potential ETWI application that would require thin or high-pemittivity dielectrics. Bypass capacitors are critical components in IC power distribution systems, as they absorb current variations and control supply voltage ripple. Implementing large value planar capacitors on-chip is extremely costly because of the economic pressure to shrink die sizes, which reduces costs and keeps power lines shorter. Currently most bypass capacitors are very expensive external, off-chip, components. A system of bypass capacitors operates over a range of frequencies, from the kilohertz to gigahertz range, and with values ranging from picofarads to microfarads. Similar to DRAM capacitors, ETWI permit a large area to be utilized while only using a small footprint on the device surface of the wafer. ETWI could connect to bypass capacitors on the backside of the wafer or be used for bypass capacitors themselves. The back of the wafer could be connected to ground through the package, and thus be used as a ground for the ETWI bypass capacitors. Alternating many layers of conductor and dielectric can be used to increase the capacitance density. This approach also has the potential to increase the density of wire ETWI applications, as multiple signals could be passed through the same via. For the capacitor application, a conformal thin film, such as tantalum oxide, would have an elevated dielectric permittivity of up to ten times greater than that of oxide and would help to increase the potential capacitance density [106, 107]. A potential challenge for this application would be in controlling the leakage current characteristics of films only a few hundred angstroms thick. The roughness of the TMICP etch would also need to be reduced dramatically, but many researchers are working on this issue because of the need for smooth sidewalls for optical MEMS applications.

There are a variety of processes for high-temperature compatible conductors worth investigating for ETWI fabrication. To reduce the resistance an order of magnitude below that of doped polysilicon, tungsten can be integrated. As described in Chapter 5, we did not pursue this because we were limited by the regulations of our fabrication facility, but the IC industry routinely combines polysilicon and tungsten onto the same wafers. Amorphous polysilicon is a thin film that can be grown as very large grains, which results in transistor device quality surfaces [108]. For ETWI applications where the 1/f noise characteristics of traditional CVD polysilicon films are unsatisfactory,

this large grain polysilicon process has the potential to be quieter because reducing the number of grain boundaries is associated with reduced low frequency noise in polysilicon [98]. Similarly, polycrystalline silicon germanium, a high-temperature compatible, conformal thin film used in IC and MEMS processes [109], has been shown to have quieter 1/f noise characteristics than polysilicon because of reduced barrier potentials [110]. Polycrystalline silicon germanium also has the advantage that it is deposited at a low temperature (less than 450°C), so it may have applications in post-process ETWI fabrication. Instead of using CVD polysilicon, epitaxial polysilicon, where polysilicon is grown from a seed layer, is a candidate for filling vias, as thick layers (over 10 μm), can be grown ten times more quickly than with CVD techniques [111]. This reduces manufacturing costs and makes larger diameter via designs more easy to fill.

6.2.2. ETWI Integration and Manufacturing

This thesis focused on pre-process ETWI for released sensor arrays. However, as described in detail in Chapter 1, ETWI have broad applications for both IC and MEMS devices. One of the most compelling motivations described is the potential to integrate an IC process onto a wafer with pre-processed ETWI, with minimal change to the IC process because the ETWI wafer is high-temperature compatible and planar. While the pre-process approach used in this work has been shown to be useful in the research laboratory, to become attractive to industry, important issues concerning integration and manufacturability need to be addressed.

Industrially manufactured electronics need to be robust. Thermal cycling, stress, and reliability issues related to the filled ETWI in this work have not yet been studied for this scale geometry. However, smaller polysilicon contact plugs (a few microns deep) with similar or greater aspect ratios have been successfully integrated with standard IC processes [112, 113]. Previous studies suggest the thermal strain mismatch between silicon and polysilicon is negligible, so stresses are expected to come from oxide mismatches and polysilicon internal stress [114]. This will have implications for the practical limits of film thicknesses and thus the achievable electrical performance.

Cost is an issue industry must use to evaluate the manufacturability of a process. The pre-process ETWI requires etching through the entire substrate, which must be thick

enough to support the wafer through the mechanical stresses of future processing. The TMICP etching technology used in this work required approximately 300 minutes of etching for the via. Such long processes are common in thin film deposition, where hundreds of wafers are processed in parallel, but for a single wafer machine like the TMICP tool, this is considered extremely costly. From a business perspective, the cost of the process should be evaluated in relation to the benefit, which may still be positive after such a long etch. However, single wafer plasma etches currently used in industry are generally at the most tens of minutes long, which means acceptance of such a process may require overcoming psychological barriers, even if the business argument is sound.

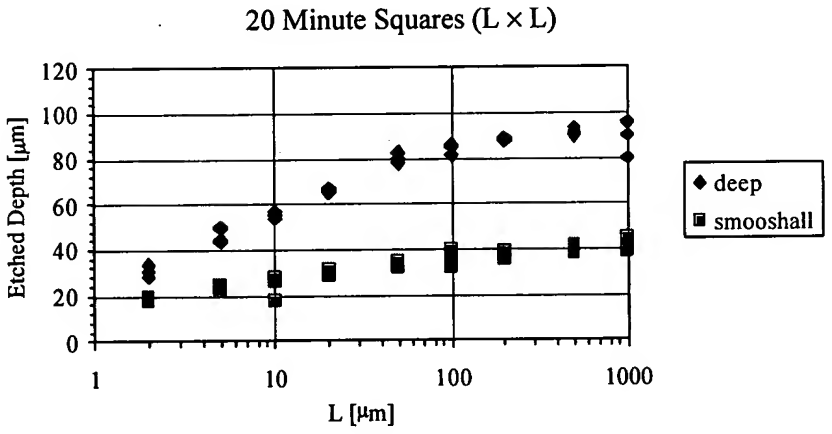
The cost of the etching process can be reduced by increasing the etch rate or decreasing the etch depth. Etch rate is critical because it determines the time the wafer is in the etcher and thus the cost of the process. Efforts underway to increase the etch rate have been previously described. Ultimate rates of over 10 μm/min are theoretically possible, but to maintain a high aspect ratio, rates only a factor of 2 or 3 faster than those demonstrated in this work are likely with current technology [67-69]. This is compounded by the fact that manufacturing processes use larger diameter wafers that are thicker; 300 mm wafers that are used by state-of-the-art IC facilities are 700 μm thick.

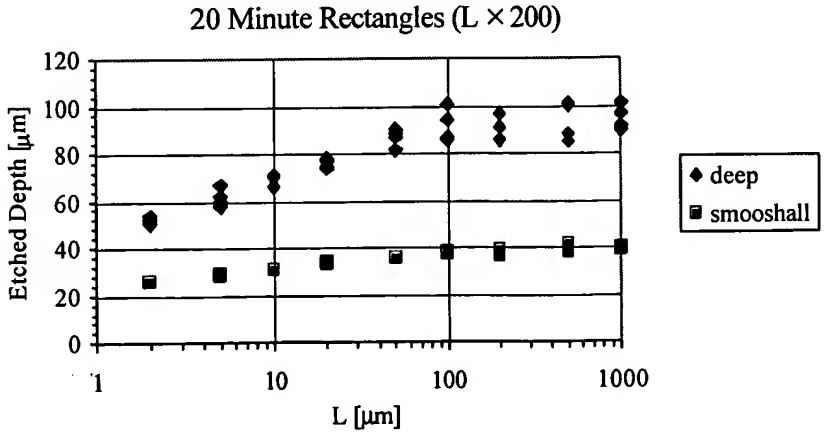
Using a thinner wafer that requires a shallower etch is thus an attractive approach for reducing the cost of the etch. This can be accomplished by adding a wafer thinning process after the final device fabrication. The ETWI could be fabricated on the thick substrate, but the via would only go a fraction of the depth. Currently IC chips are thinned before packaging to about 200 μm for thermal expansion reasons, so this would be a reasonable depth. The design curves of Figure 5-2 would vertically shift down by a factor of two. This would also reduce the possible footprint because the required aspect ratio decreases. The challenge would then be to control the thinning so as to stop on the ETWI, as well as to leave contacts that are accessible and isolated without performing future lithography. Tru-Si is a company which is pursuing such an approach using isotropic etching and metal deposition for a post-process ETWI with a millimeter diameter footprint [51]. Tru-Si uses a wafer thinning etch which is selective, and thus stops on oxide. Such an approach could be combined with the pre-process ETWI to fabricate high-density ETWI with diameters down to 10 μm.

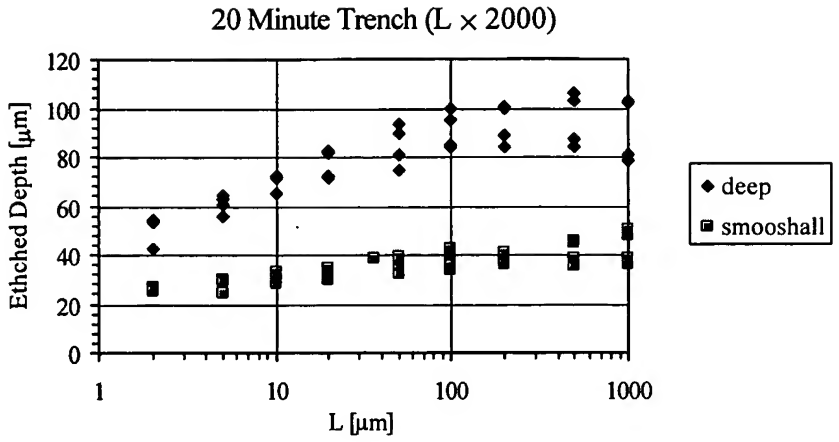
A final challenge for acceptance of pre-process ETWI is the fear all manufacturing lines have for contamination. Most semiconductor manufacturing processes require very tight control over the materials brought into a facility, as contamination can reduce yields and be extremely costly to eradicate. New, polished, silicon wafers are the standard starting point for manufacturing lines. Allowing wafers to enter the line which have already been processed elsewhere is very unorthodox, and probably unheard of for many IC fabrication facilities. Thus the acceptance of pre-process ETWI on a large scale to reduce costs might require the manufacturer of the rest of the device to also fabricate the ETWI. Despite the potential business challenges for mass produced pre-process ETWI, pre-process ETWI have a promising future for making significant technical contributions in the ever important fields of IC and MEMS.

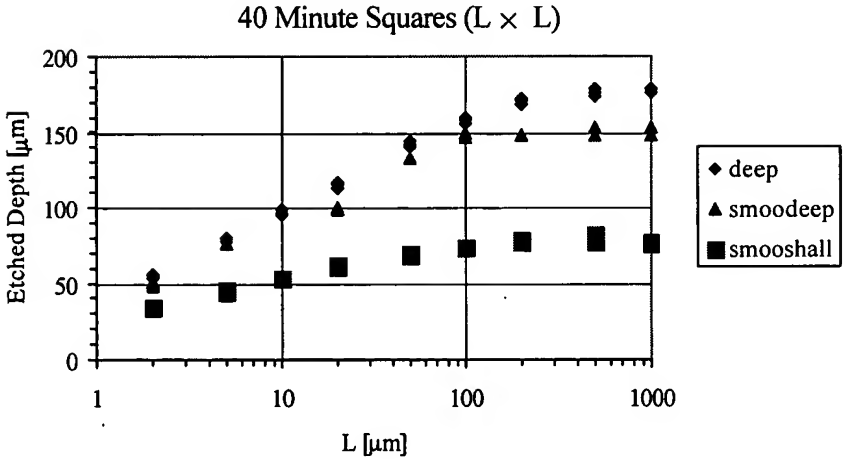
Appendix A: Complete TMICP Etch Characterization Data

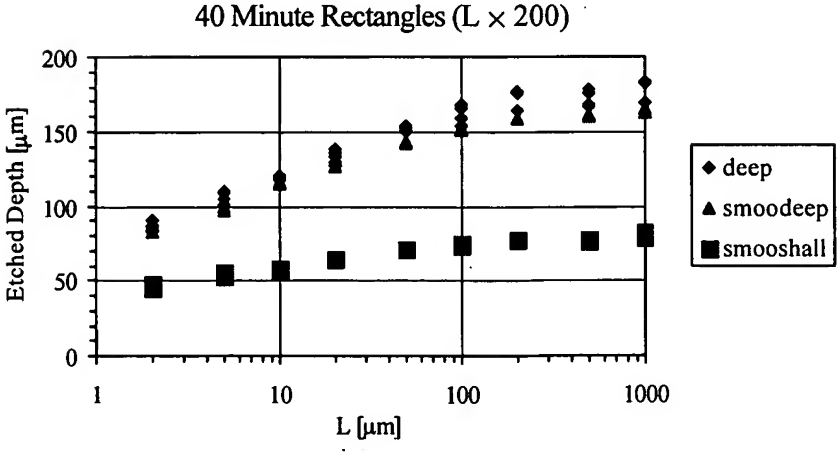
This appendix contains the detailed summary of the etch depth data from the TMICP etch characterization experiment described in Chapter 2. Three recipes were used: DEEP, SMOODEEP, and SMOOSHALL (see Table 2-1). Three different times were used: 5, 20, 40 and 80 minutes. Three different shapes were used: squares (L × L), rectangles (L × 200 μm), and trenches (L × 2000 μm). Two different pattern densities were used: 5% and 15%, and measurements were taken at the middle and edge of the wafer. Note the density is 15% unless noted otherwise. For L = 2, 5 and 10 μm vias, mask erosion effects produced side walls that were not as vertical as larger vias.

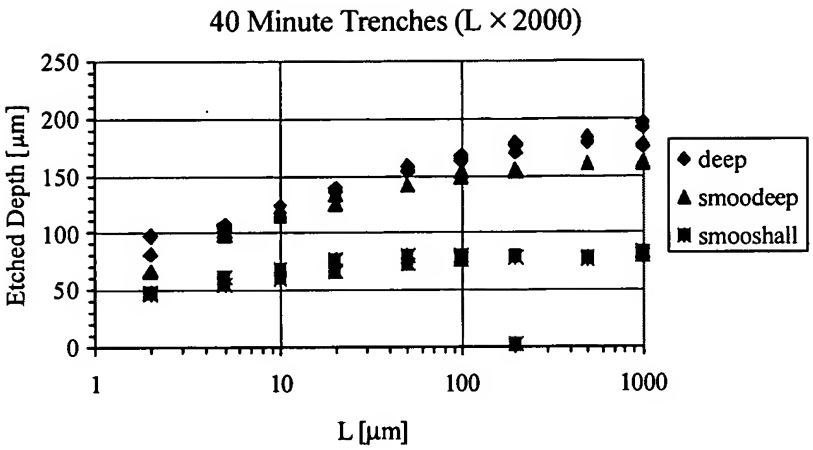


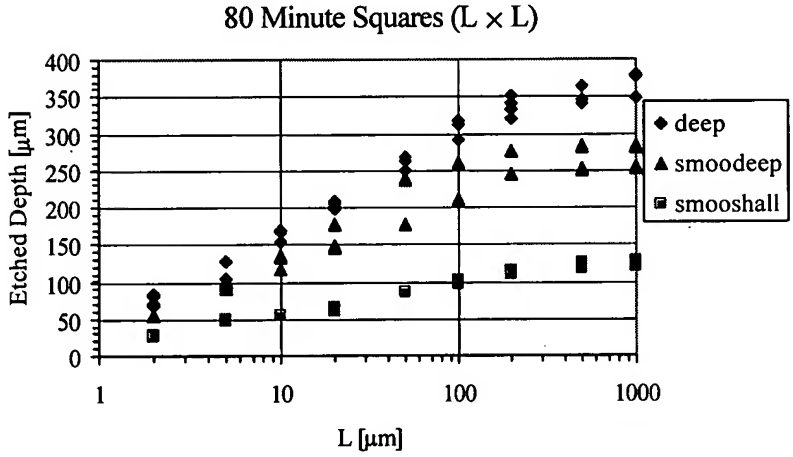


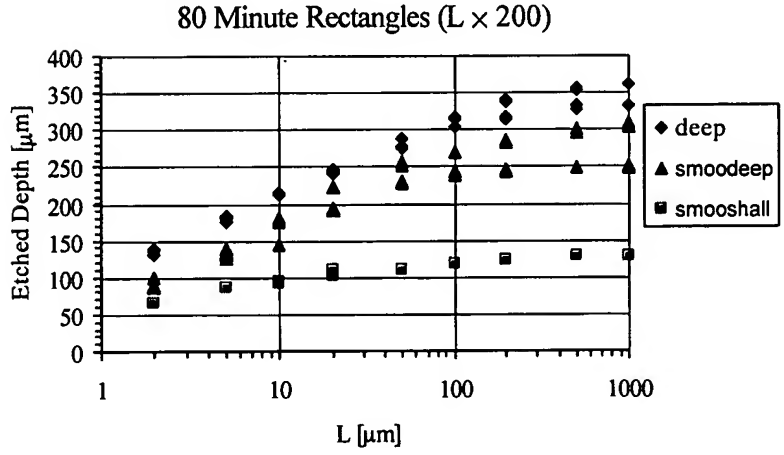

20 Minute Trench (L × 2000)
Ethched Depth [µm]
120
100
80
60
40
20
0
1
10
100
1000
L [µm]
deep
smooshall

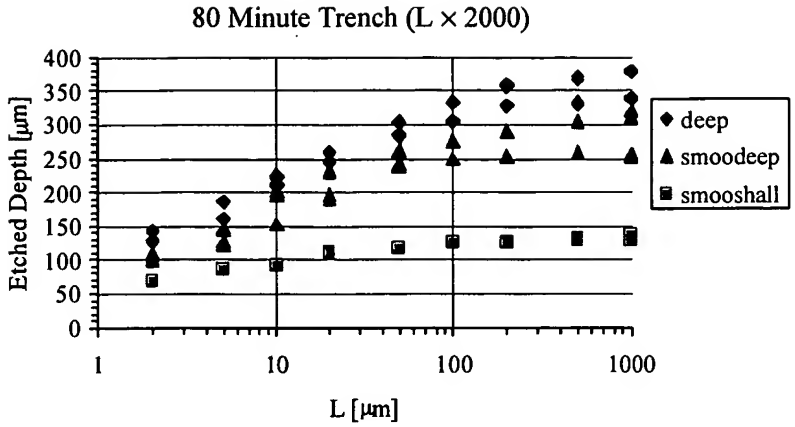

40 Minute Squares (L × L)
Etched Depth [µm]
200
150
100
50
0
1
10
100
1000
L [µm]
deep
smoodeep
smooshall

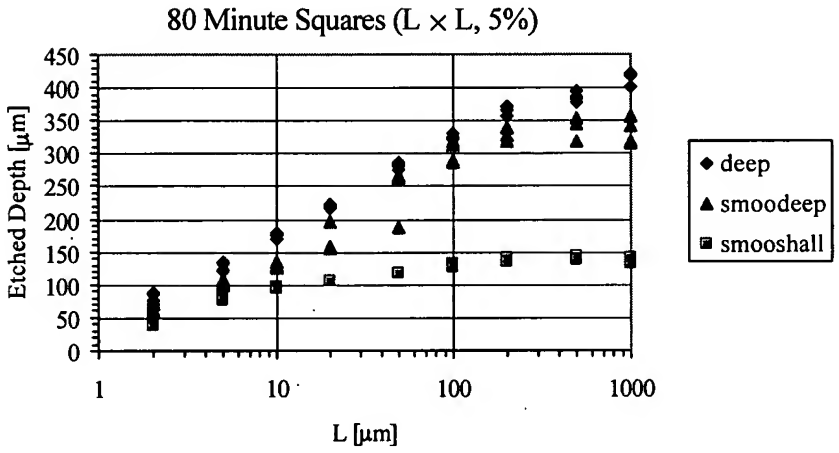

40 Minute Rectangles (L × 200)
Etched Depth [µm]
200
150
100
50
0
1
10
100
1000
L [µm]
deep
smoodeep
smooshall

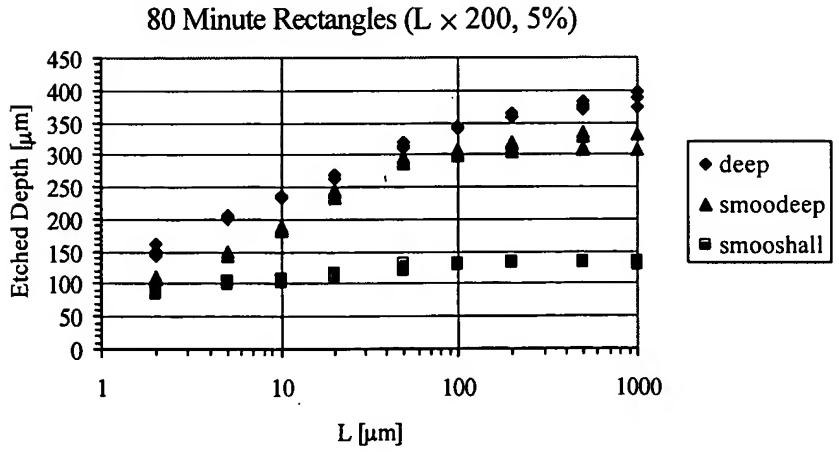

40 Minute Trenches (L × 2000)
Etched Depth [μm]
250
200
150
100
50
0
1
10
100
1000
L [μm]
deep
smoodeep
smooshall

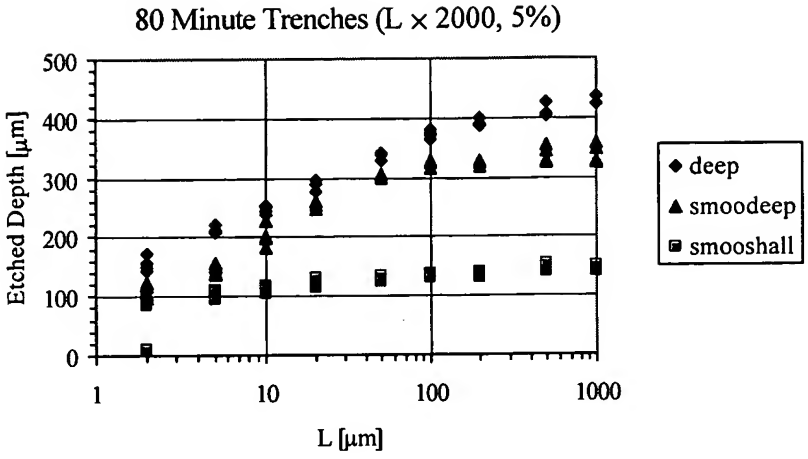

80 Minute Squares (L × L)
Etched Depth [μm]
400
350
300
250
200
150
100
50
0
1
10
100
1000
L [μm]
deep
smoodeep
smooshall


80 Minute Rectangles (L × 200)
Etched Depth [μm]
400
350
300
250
200
150
100
50
0
1
10
100
1000
L [μm]
deep
smoodeep
smooshall

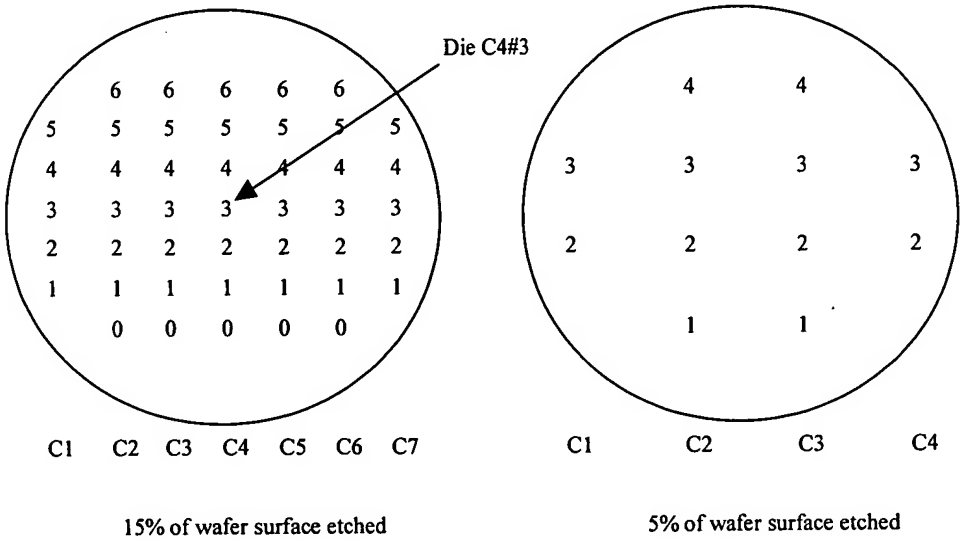

80 Minute Trench (L × 2000)
Etched Depth [µm]
400
350
300
250
200
150
100
50
0
1
10
100
1000
L [µm]
deep
smoodeep
smooshall


80 Minute Squares (L × L, 5%)
Etched Depth [µm]
450
400
350
300
250
200
150
100
50
0
1
10
100
1000
L [µm]
deep
smoodeep
smooshall


80 Minute Rectangles (L × 200, 5%)
Etched Depth [µm]
450
400
350
300
250
200
150
100
50
0
1
10
100
1000
L [µm]
deep
smoodeep
smooshall



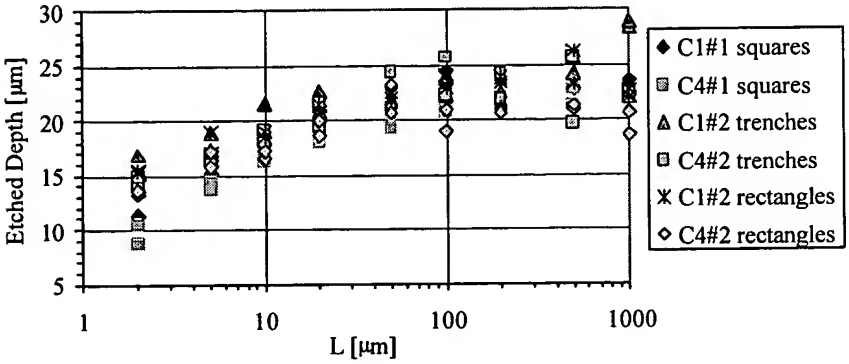
For the following plots, detailed information on nonuniformity is included. The measurements are taken from different spots on the wafer with the position based on coordinates from the following grid.



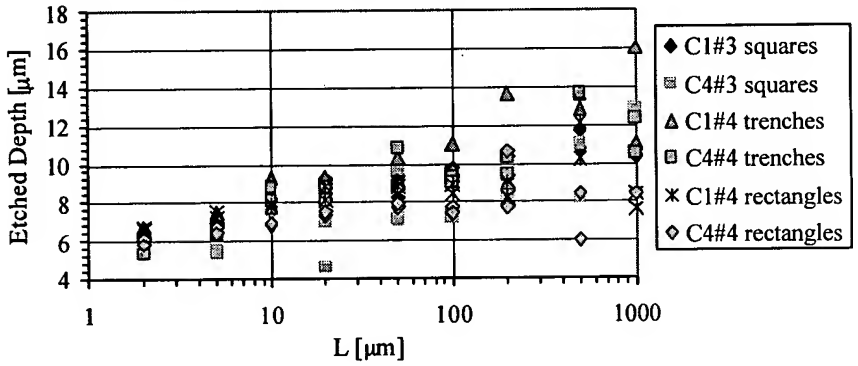
15% of wafer surface etched

5% of wafer surface etched

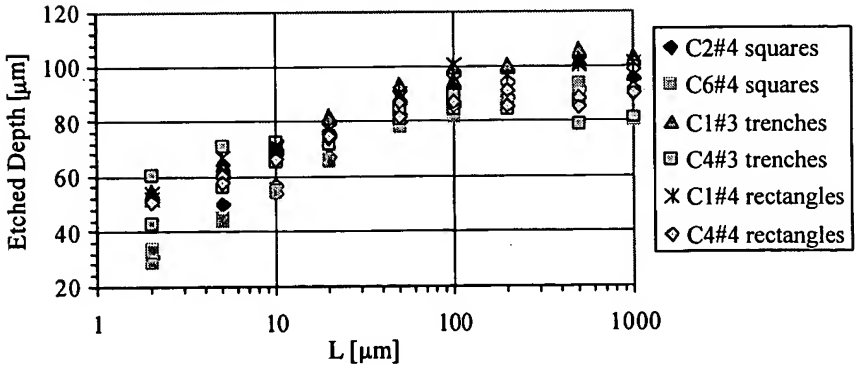
All Geometries 5 Minute DEEP Graph



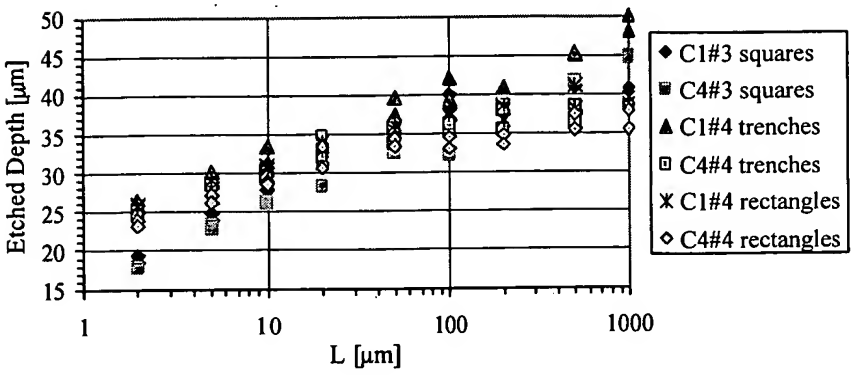
All Geometries 5 Minute SMOOSHALL Graph



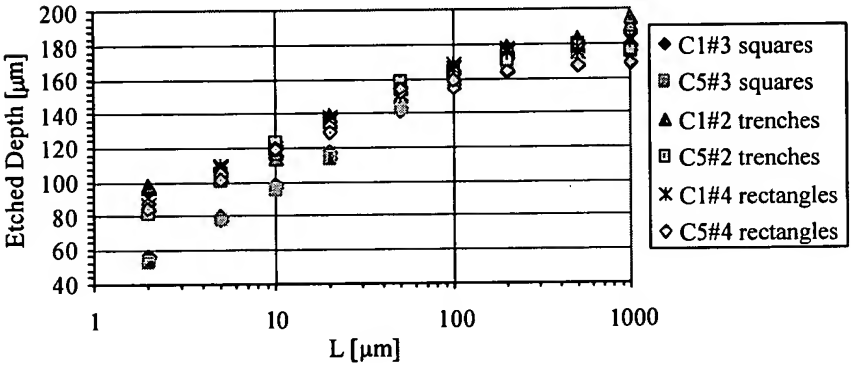
All Geometries 20 Minute DEEP Graph



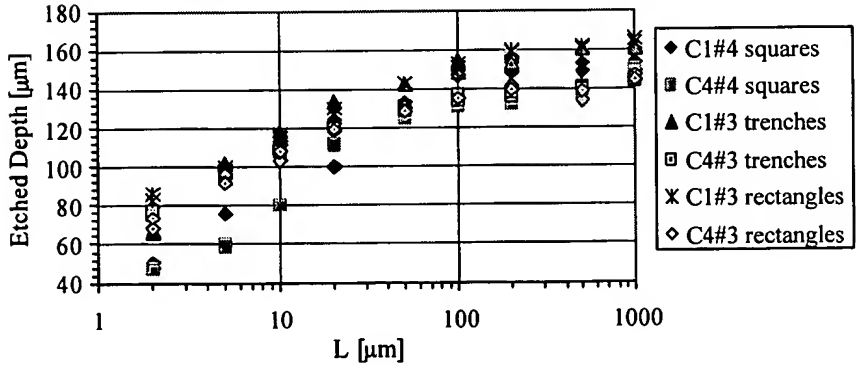
All Geometries 20 Minute SMOOSHALL Graph



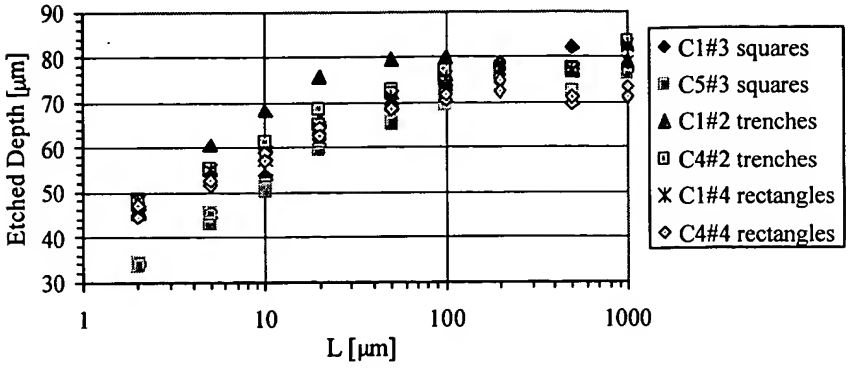
All Geometries 40 Minute DEEP Graph



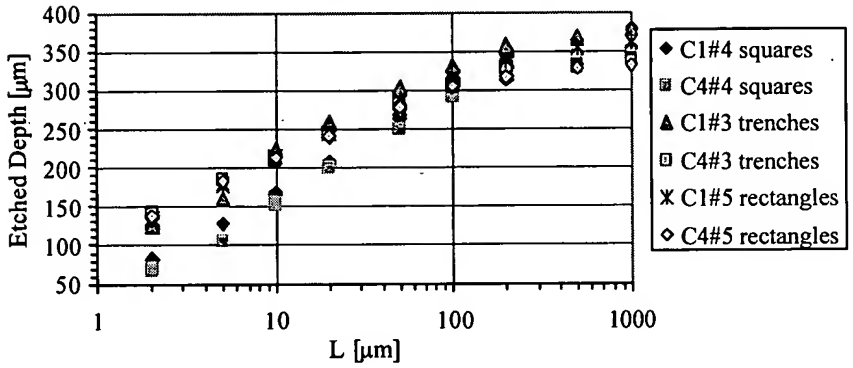
All Geometries 40 Minute SMOODEEP Graph



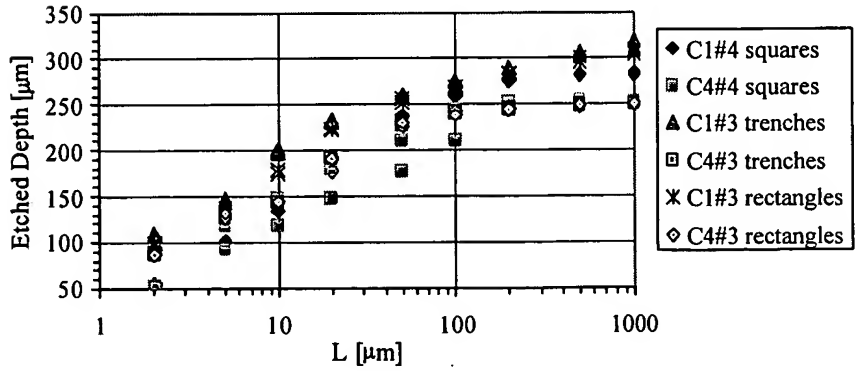
All Geometries 40 Minute SMOOSHALL Graph



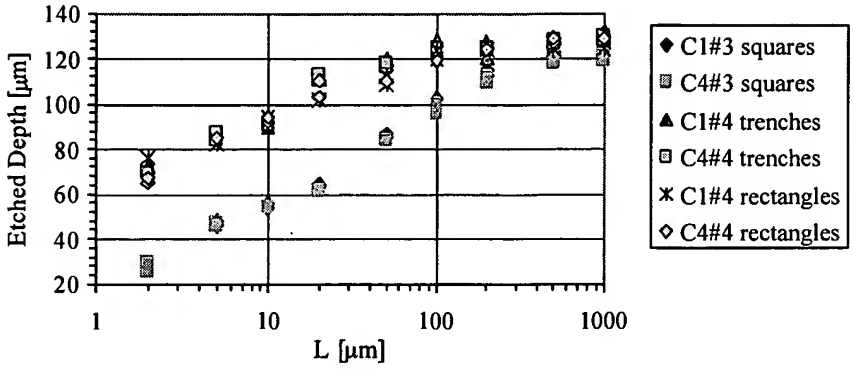
All Geometries 80 Minute DEEP Graph



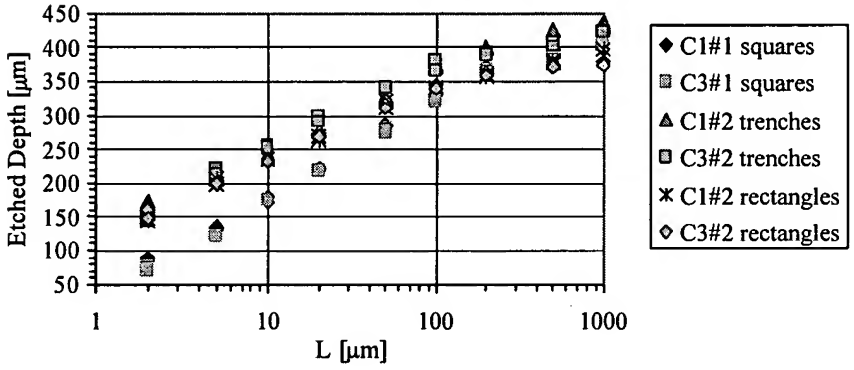
All Geometries 80 Minute SMOODEEP Graph



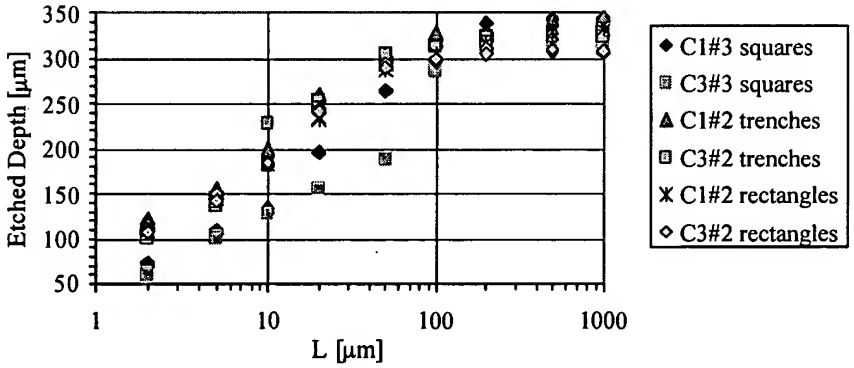
All Geometries 80 Minute SMOOSHALL Graph



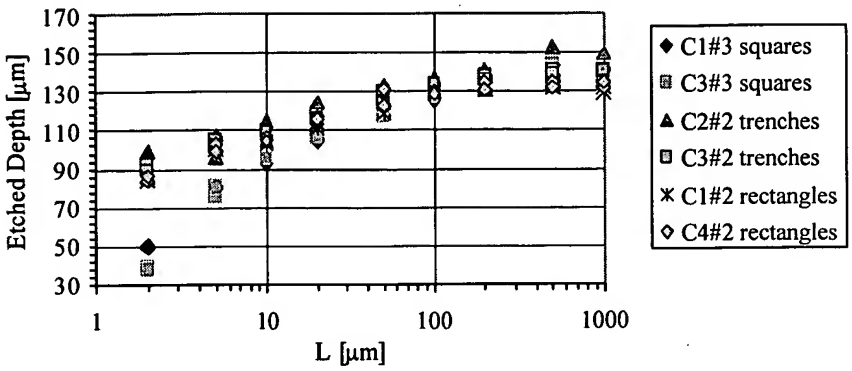
All Geometries 80 Minute (5%) DEEP Graph



All Geometries 80 Minute (5%) SMOODEEP Graph



All Geometries 80 Minute (5%) SMOOSHALL Graph



Appendix B: 2D Array Process Flow Details

This is the detailed process used for the fabrication of 2D arrays of piezoresistive cantilevers with integrated tungsten electrical through-wafer interconnects (see Figure 4.10). The instructions assume fabrication at the Stanford Nanofabrication Facility.

0. *Starting Material*
SOI's with 20μm thick top Si, 1.9μm buried oxide, double polished, 1.5μm oxide on back
Scribe
Scribe clean
Wbnonmetal piranha
Strip backside oxide
Wbnonmetal 6:1 BOE long time -rinse, spin dry
1. *Form Tips (take 3+ dummies for SEM)*
Grow oxide tip mask
Oxidation diffusion clean
Wbdiff sulfuric/peroxide, HF, HCl/peroxide
Grow 1μm thermal oxide
Tylan tubes WET1100 2h30m
Pattern Resist Tip mask
Singe @150C for 1hr
Coat 1μm resist
Svgcoat prog#1
Expose with tip mask
Karlsuss low vacuum mode, 2.2sec, 40μm gap, 4sec purge etc.
Make sure squares have corners, watch for current overdrives
Develop
Svgdev prog#1
Etch Oxide
Wbnonmetal 6:1 BOE 20min, rinse, spin dry
Strip resist
Wbnonmetal piranha, rinse
Native oxide clean
Wbnonmetal 50:1 HF for 3min, rinse, spin dry to prevent grass
Pattern Tips
Isotropic etch
Drytek2 sf6 150ccm, 357w, 150mtorr, 230coil, 83 cap
Stop before any caps fall off, but neck ~1μm; ~300-400s
Anisotropic etch
LAM prog#1 (15mtorr, 250W, 150 HBr, 5 O2) ~ 15min
SEM test wafer
Measure neck width and surface roughness across wafers
Strip oxide caps
Wbnonmetal 6:1 BOE 20min, dump rinser
Strip passivation layer
Wbnonmetal piranha 30min, dump rinser, spin dryer
Oxidation Sharpen Tips
Oxidation diffusion clean

Wbdiff sulfuric/peroxide, HF, HCl/peroxide

Grow thermal oxide – thickness depends on neck/grass measurement

Wet950 5+ hrs for 1-1.5μm - High temp to make sure neck cut off.

Strip oxide on inspection test wafer only

wbnonmetal 6:1 BOE 10-20min, dump rinser, spin dryer

Make sure sharp, measure cantilever surface roughness, return half of wafer for next oxidation if necessary

Thin oxide to 1000A (on full lot)

wbnonmetal 6:1 BOE (time to get to 1000A for implant mask), dump rinser, spin dryer - want thin to implant through

2. Global Alignment Marks

Pattern global alignment marks

Singe @150C 15min.

Coat resist 18μm

Svgcoat modified prog4, AZ4620 spin at 1krpm (very thick over tips)

With hmds, 200sec hotplate @105C or Bake 1hr at 90C in oven

Expose with global align mask

Karlsuss soft contact mode, 60sec exp, 20sec wait, 60sec exp

Use Al foil on mask to only expose alignment mark area of wafer

Develop

Svgdev prog#6 Mf319, with hotplate bake#2 or by hand ~10min

Etch mask into oxide

Wbnonmetal 6:1 BOE ~min (time for 1000A oxide), dump rinser, spin dry

Measure oxide thickness on back (leave for ETWI stop)

Etch marks into Si

drytek2 "Si etch" for 5min

Strip resist

Acetone, isopropanol, spray first to remove majority of resist

Wbnonmetal piranha 20min, dump rinser, spin dry

3. Piezoresistors

Pattern implant resist mask

Singe @150C 15min.

Coat resist 18μm

Svgcoat modified prog4, az4620 spin at 1krpm (very thick over tips)

With hmds, 200sec hotplate @105C or Bake 1hr at 90C in oven

Expose with piezoresistor mask

Karlsuss soft contact mode, 60sec exp, 20sec wait, 60sec exp

Develop

Svgdev prog#6 Mf319, with hotplate bake#2 or by hand ~6min

Postbake

90C for 1hr Bake resist more for implant

Implant (through 1000A oxide)

April or Ion Implant services

Boron, 5e14/cm2, 80keV – designed for sensitive piezoresistor

Strip resist

Matrix 3-5min each

Acetone, isopropanol spray to remove majority of resist

Wbnonmetal piranha 20min, dump rinser, spin dry

Pattern contact implant resist mask

Singe @150C 15min.

Coat resist 18μm

Svgcoat modified prog4, AZ4620 spin at 1krpm (very thick over tips)

With hmds, 200sec hotplate @105C or Bake 1hr at 90C in oven

Expose with contact mask

Karlsuss soft contact mode, 60sec exp, 20sec wait, 60sec exp

Develop

Svgdev prog#6 Mf319, with hotplate bake#2 or by hand ~6min

Postbake

90C for 1hr Bake resist more for implant

Implant (through 1000A oxide)

April or Ion Implant services

Boron, 5e15/cm2, 40keV – heavy for ohmic contact

Strip resist

Matrix 3-5min

Acetone, isopropanol spray to remove majority of resist

Wbnonmetal piranha 20min, dump rinser, spin dry

No RTA needed because dopants will be activated during LPCVD runs

Strip oxide

6:1 BOE, rinse, spin dry

4. Through Wafer Interconnects

Pattern topside ETWI resist/oxide mask

Coat resist 18μm

Headway spin 600 rpm,

Bake

90C oven 1hr resist up

Expose with ETWI mask on both sides

Karlsuss low vacuum, proximity mode, 30sec exp, 20sec wait, 30sec exp

Develop

Mf319 by hand, use automatic rotator at 2Hz, ~5min

Etch ETWI from top

Etch top Si

STSetch smooshall ~5min time carefully to avoid oxide interface explosion

Strip top resist

Acetone, piranha

Etch buried oxide

Wbnonmetal 6:1 BOE, etch backside oxide

Pattern backside ETWI resist mask (no oxide mask) – leave front resist for tip protection

Coat resist both sides 18μm

Headway tipside and then back, spin 600rpm, 5krpm kick to thin edge bead

Bake

90C oven 1hr back side up

Expose with ETWI mask

Karlsuss low vacuum, proximity mode, 30sec exp, 20sec wait, 30sec exp

Develop

Mf319 by hand, use automatic rotator at 2Hz, ~5min

Bake for sts

90C oven 1hr

Etch ETWI from back of wafer

Etch Si deep to meet top hole

STSetch polyimide tape to cover resist blemishes, both sides

etch alignment marks: 1min of deep

through: ~200min "deep

clean edge: ~20min "soi-2"

Look for light through – don't overetch too much

Strip resist

Acetone, isoproponal spray for to remove majority of resist

Wbnonmetal piranha ~1hr+ until very clean, dump rinser, spin dry

Deposit ETWI thin films

a) 0.5μm LTO (for tip protection)

b) 0.3μm nitride isolation layer

c) ~1μm poly sticking layer

Schedule tubes back to back to skip 2nd and 3rd diff clean

LPCVD diffusion clean
Wbdiff sulfuric/peroxide, HCl/peroxide, HF -clean oxide 2 dummies too
Tylanbpsg LTO400 20min - want 0.5μm
- remove dummy 1 for the tylanpoly run
-don't place dummy 2 in this run
Tylannitride sin5.2 3hr (8800A) -take dummy 2 for thickness test
Tylanpoly polyemit 88min (9800A) -add dummy 1 oxide for thickness check
Pattern contact hole resist mask
Coat resist 16μm
headway 600 rpm, pour AZ4620 while still, spin for 15sec at 1krpm,
store upside down immediately to avoid thinning at corners
Bake
90C oven 1hr -resist upside down! Expose with contact mask
Karlsuss soft contact mode, 30sec exp, 20sec wait, 30sec exp
Develop
By hand mf319 ~6min, keep vertical, make sure very clear
Etch contact poly/nitride
Drytek2 "nitride etch" 5(poly)+5(nitride) min
-stop on contact oxide, test dummy first
Strip resist
Acetone, isoproponal spray for to remove majority of resist
Wbnonmetal piranha ~1hr+ until very clean, dump rinser, spin dry
Etch contact oxide
wbnonmetal 6:1 BOE ~4-6min
-make sure contact and native oxide gone
-do after resist gone so no wetting problem
Strip native oxide
wbnonmetal 6:1 BOE 3min -dump rinse, spin dry (no blow)
-strip immediately before spectrum
CVD tungsten
Spectrum standard program 30min
- clean chamber with thick oxide wafer, run dummies
- should measure ~0.3ohm/sq
- flip wafer
standard program 30min - for back of wafer
- careful of tips!!!

5. Front Metal

Pattern frontside metal resist mask
Coat resist 16μm
headway 1krpm, pour AZ4620 while still, spin for 15sec at 1krpm,
store upside down immediately to avoid thinning at corners
Bake
90C oven 1hr -upside down!
Expose with front metal mask
Karlsuss soft contact
Develop
Mf319 by hand, keep vertical
-rinse by hand, blow dry, make sure all patterns adhered
UV bake 20min, Dektak resist thickness check
Etch frontside tungsten/poly/nitride
Drytek2 "nitride etch" 5(W)+5(poly)+5(nitride) min
-stop on oxide, dummy first
Etch frontside oxide
Wbmetal 6:1 BOE 4-6min -strip tip protection oxide, look at tips
Strip resist
Acetone, isopropanol spray to remove majority of resist

Wbmetal EMT130-T ~5min, dump rinser, spin dry
PRS1000 ~5min, dump rinser(2x), spin dry

6. Back Metal

Clean for aluminum
Wbmetal PRS-1000 clean then rinse, dry, rinse, dry.
Sputter aluminum
Gryphon 0.5μm, use manual palette load to protect tips
Pattern backside metal resist mask
Coat resist 16μm
headway 1krpm, pour AZ4620 while still, spin for 15sec at 1krpm,
store upside down immediately to avoid thinning at corners
Bake 90C oven 1hr -upside down!
Expose back with back metal mask
Karlsuss 60sec 2x
Develop
Mf319 by hand, keep vertical
-rinse by hand, blow dry, make sure all patterns adhered
UV bake 20min - make sure no bubbles, Dektak resist thickness check
Protect tips on underside
Coat resist 16μm
headway 1krpm, pour AZ4620 while still, spin for 15sec at 1krpm,
store upside down immediately to avoid thinning at corners
Bake 90C oven 1hr -upside down!, inspect to make sure no bubbles on either side
Etch backside aluminum
Wbmetal aluminum etch, rinse, spin dry
Etch backside tungsten/poly/nitride
Drytek2 "nitride etch" 5(W)+5(poly)+5(nitride) min
-stop on oxide, dummy first
Etch backside oxide
Wbmetal 6:1 BOE 4-6min -strip back oxide since don't need for back release
Strip resist
Acetone, isopropanol spray to remove majority of resist
Wbmetal EMT130-T ~5min, dump rinser, spin dry
PRS1000 ~5min, dump rinser(2x), spin dry

7. Etch Cantilevers

Pattern cantilever resist mask
Coat resist 16μm
headway 1krpm, pour az4620 while still, spin for 15sec at 1krpm,
store upside down immediately to avoid thinning at corners
Bake 90C oven 1hr -upside down!
Expose back with cantilever mask
Karlsuss low vacuum, proximity, for good sidewalls
Develop
Mf319 by hand, keep vertical -rinse by hand, blow dry
UV bake 20min - make sure no bubbles!, Dektak resist thickness check
Etch cantilevers
STSetch SOI-2 for 1min per 1μm device thickness (5-10μm)
-nanospec and Dektak till get only oxide
Strip resist
Acetone, isopropanol spray to remove majority of resist
Wbmetal EMT130-T ~5min, dump rinser, spin dry
PRS1000 ~5min, dump rinser(2x), spin dry

8. Release Cantilevers

Pattern cantilever resist mask
Coat backside with resist 16μm

headway 1krpm, pour AZ4620 while still, spin for 15sec at 1krpm,
store upside down immediately to avoid thinning at corners

Bake 90C oven 1hr -upside down!

Expose back with back metal mask

Karlsuss 60sec 2x

Develop

Mf319 by hand, keep vertical -rinse by hand, blow dry

UV bake 20min - make sure no bubbles!

Protect tips on underside

Coat resist 16μm

headway 1krpm, pour AZ4620 while still, spin for 15sec at 1krpm,
store upside down immediately to avoid thinning at corners

Bake 90C oven 1hr -upside down!, check for bubbles!

Backside release etch

STSetch deep ~2.5hr until just poke through

use Al Carrier

STSetch soi-2 ~10-20min to finish corners

Strip oxide

Wbmetal 6:1 BOE -wet first, add trident X, O2 plasma

-HF vapor last resort

-hand rinse, blow dry

Strip Resist for final release

Matrix or Drytek2 till done!

Appendix C: ETWI Process Flow Details

This is the detailed process used for the fabrication of polysilicon filled electrical through-wafer interconnects (ETWI) in silicon. These instructions are for isolated n-type ground planes surrounding an n-type signal ETWI (See Figure 5-6), and refer to equipment at the Stanford Nanofabrication Facility.

1. Scribe and Labels
Starting wafers: 4in wafers
Scribe wafers
Measure wafer thickness

Coat and pattern resist - Label mask on scribe side
Coat 1.6μm
Svgcoat prog8 (3612 resist)
Expose with label mask
Evalign (3.5sec) or Karlsuss (1min)
Develop
Svgdev prog#1
Etch label mask into silicon
Drytek2 Si etch for 10-15min
Strip resist
Wbnonmetal 20min piranha, dump rinse, spin dry

2. Pattern/etch holes
Deposit thermal oxide mask layer
Wbdiff sulfuric/peroxide, HF, HCl/peroxide
Deposit 1μm oxide
Tylan1,3 or 4 WET1000 5 hr

Coat and pattern resist/oxide on scribe side
Singe 150C 15 min
Svgcoat Coat resist 3612 for 1.6 μm at 4krpm (std program, hmds and bake)
Evalign or Karlsus ~1sec, vacuum
Svgdev Develop standard program
Clean backside dump rinse cycle
Bake for AMT 110C for 60min
Amtetcher 38min of std oxide etch (for 9400A thermal oxide)
Wbnonmetal piranha for 20min, dump rinse, spin dry

Coat and pattern resist/oxide on non-scribed side
Svgcoat Coat resist 3612 for 1.6 μm at 4krpm (std program, hmds and bake)
Evalign or Karlsus ~1sec, vacuum
Svgdev Develop standard program
Clean backside dump rinse cycle
Bake for AMT 110C for 60min
Amtetcher 38min of std oxide etch (for 9400A thermal oxide)
Wbnonmetal piranha for 20min, dump rinse, spin dry

Coat and pattern resist Hole mask on both sides

Singe 150C 15min
Coat 10μm on scribe side
Svgcoat HMDS program #1 both sides
Coat resist: spr220 spin at 1500 rpm for 60 sec, 1 sec at 5krpm for edge bead removal. Make sure no resist blemishes! (for long etch)
Bake on hotplate 120sec
Coat 10μm on non-scribe side
Svgcoat Coat resist: spr220 spin at 1500 rpm for 60 sec, 1 sec at 5krpm for
Softbake 110C oven for 90 min.
Let wafers sit in air for 10+ hours
Expose with hole mask on scribe side
Evalign or Karlsuss vacuum contact mode, 30 sec, use paper backing on chuck
Expose with hole mask on nonscribe side
Evalign or Karlsuss vacuum contact mode, 30 sec, use paper backing on chuck
Develop both sides
LDD26W by hand ~3-5min...
Don't do post bakes, as it tends to crack the resist (either immediately or in the stsetch)

Etch ETWI
Etch alignment marks
STSetch cwsdeep1 for 2 min on scribed side
STSetch cwsdeep1 for 2 min on unscribed side
Tape over alignment marks
Paint SPR220-7 over blemishes, edge of wafer and bake 90C 30-60min ONLY if litho bake was only 90C for 60min (not 110C for 90min – it will crack if it is)
Etch from scribe side halfway – tape over major resist blemishes!
STSetch cwsdeep1 ~ 210min (P=9.9, F=2.6) (shorter if wafer not 400μm)
Etch from non-scribe side halfway-tape over resist blemishes!
STSetch cwsdeep1 ~210min or until helium flow increases to ~4.5
Finish etch
Etch from scribe side, mounted wafer on a support wafer (just sitting on wafer)
STSetch cwsdeep1 ~30min (light uniform at 100x mag, d<30μm)
Etch from non-scribe side, mounted wafer on a support wafer (just sitting on wafer)
STSetch cwsdeep1 ~30min (light uniform at 100x mag, d<30μm)

Strip resist and clean etch polymer
Acetone, isopropanol and blow dry
Drytek2 5min oxygen plasma
Wbnonmetal 20min piranha
Drytek2 5min oxygen plasma

3. Deposit thin films

Deposit LPCVD oxide isolation layer
Oxidation diffusion clean – skip if just out of previous tube
Wbdiff sulfuric/peroxide, HF, HCl/peroxide
Deposit 1μm oxide
Tylan1,3 or 4 WET1000 for 5hr

Deposit LPCVD polysilicon signal conduction layer
LPCVD diffusion clean – skip if just out of previous tube
Wbdiff sulfuric/peroxide, HCl/peroxide, HF
Deposit ~3μm polysilicon
Tylan9 POLYEMIT for 3h30m
Inspect

Make sure light still through all holes

Dope polysilicon ground plane phosphorus

LPCVD diffusion clean – skip if just out of previous tube

Wbdiff sulfuric/peroxide, HCl/peroxide, HF

Phosphorus dope poly

Tylan6 POCL (in directory "predep") for 30min

Deposit LPCVD oxide isolation layer

Clean phosphosilicate glass

Wbdiff 6:1 BOE ~2min...

Oxidation diffusion clean – skip if just out of previous tube

Wbdiff sulfuric/peroxide, HF, HCl/peroxide

Deposit 2μm oxide

Tylan1,3 or 4 WET1150 for 7hr

Deposit LPCVD polysilicon signal conduction layer

LPCVD diffusion clean – skip if just out of previous tube

Wbdiff sulfuric/peroxide, HCl/peroxide, HF

Deposit ~3μm polysilicon

Tylan9 POLYEMIT for 3h30m

Inspect

Make sure light still through all holes

Dope polysilicon ground plane phosphorus

LPCVD diffusion clean – skip if just out of previous tube

Wbdiff sulfuric/peroxide, HCl/peroxide, HF

Phosphorus dope poly

Tylan6 POCL (in directory "predep") for 30min

Fill ETWI holes

Clean borosilicate glass off of poly and diff clean

wbdiff 20:1BOE for 2 min minimum....

Wbdiff sulfuric/peroxide, HCl/peroxide

Deposit 3+μm of poly to fill (assuming started with 20μm diameter hole)

Tylan9 POLYEMIT for 4hr

Dope surface polysilicon with boron or phosphorus

LPCVD diffusion clean – skip if just out of previous tube

Wbdiff sulfuric/peroxide, HCl/peroxide, HF

Phosphorus dope poly

Tylan6 POCL (in directory "predep") for 30min

Drive in boron or phoshporus

LPCVD diffusion clean if just out of previous tube

Wbdiff sulfuric/peroxide, HCl/peroxide, HF

Anneal

Tylan1,2 or 4 1000AN for 1 hr

Clean borosilicate glass off of poly and diff clean

Wbnonmetal 20:1BOE for 2 min minimum....

Wbdiff sulfuric/peroxide, HCl/peroxide

4. Pattern top signal and bottom poly

Coat both sides with 10μm resist

Headway2 spr220 resist 1.5krm

Softbake 110C oven for 90 min.

Let wafers sit in air for 10+ hours

Expose scribed side with signal mask

Evalign or Karlsuss vacuum contact mode, 30 sec, use paper backing on chuck

Expose nonscribed side with bottommetal mask

Evalign or Karlsuss vacuum contact mode, 30 sec, use paper backing on chuck
Develop
LDD26W by hand
Etch top poly
Drytek2 Si etch for 15-20 min stopping on oxide
Etch backside poly
Drytek2 Si etch for 15-20 min
Strip resist
Acetone, isopropanol and blow dry
Wbnonmetal 20min piranha

5. Pattern top-ground plane
Coat both sides with 10μm resist
Headway2 spr220 resist 1.5krm
Softbake 110C oven for 90 min.
Let wafers sit in air for 10+ hours
Expose scribed side withTOP-GND (surrounds interconnects)
Evalign or Karlsuss vacuum contact mode, 30 sec, use paper backing on chuck
Expose non-scribed side with TOP-GND (surrounds interconnects)
Evalign or Karlsuss vacuum contact mode, 30 sec, use paper backing on chuck
Develop
LDD26W by hand
Etch oxide both sides
Wbononmetal 6:1 BOE for 10-15min, dumprinse, spin dry
Etch ground poly on scribed side
Drytek2 polyetch 20min stopping on oxide
Etch ground poly on unscribed side
Drytek2 polyetch 20min
Strip photoresist
Acetone
Wbnonmetal piranha, dumprinse, spin dry

6. Passivate and Open Oxide in Contact Pads and Dope: substrate, ground poly, and signal poly
Deposit resistor passivation LTO
LPCVD diffusion clean
Wbdiff sulfuric/peroxide, HCl/peroxide, HF
Deposit 1-2μm LTO
Tylanbpsg LTO400 time Load wafers every other slot so both sides deposited
Deposit polysilicon mask for thick oxide etching
Coat both sides with 10μm resist
Headway2 spr220 resist 1.5krpm
Softbake 110C oven for 90 min.
Let wafers sit in air for 10+ hours
Expose scribed side with PAD-LIFT
Evalign or Karlsuss vacuum contact mode, 30 sec, use paper backing on chuck
Develop
LDD26W by hand
Etch oxide
Wbnonmetal 6:1 BOE ~20-30min, dumprinse, spindry
Make sure all pads clear!
Strip photoresist
Acetone
Wbnonmetal piranha, dumprinse, spin dry

Dope surface polysilicon with boron or phosphorus

LPCVD diffusion clean – skip if just out of previous tube
Wbdiff sulfuric/peroxide, HCl/peroxide, HF
Phosphorus dope poly
Tylan6 POCL (in directory "predep") for 30min
Clean phosphosilicate glass off of poly and diff clean
Wbnonmetal 20:1BOE for 2 min minimum

7. Deposit Aluminum and anneal

Sputter Aluminum
Wbmetal PRS1000
HF dip to clean contact, dumprinse, spin dry
Gryphon argon sputter etch, 1-2μm of aluminum...

Coat both sides with 10μm resist
Headway2 spr220 resist 1.5krpm
Softbake 110C oven for 90 min.
Let wafers sit in air for 10+ hours
Expose scribed side with PAD-MET
Evalign or Karlsuss vacuum contact mode, 30 sec, use paper backing on chuck
Develop
LDD26W by hand
Etch Aluminum
Wbmetal aluminum etch, time, dump rinse, spin dry
Clean up Al/Si etch
Drytek2 Freckle etch, few min
Strip resist
Acetone, isopropanol and blow dry
Wbnonmetal 20min piranha

Forming Gas Anneal
Wbmetal PRS1000
Tylanfga FGA400 2hrs

Publications

Refereed Publications

E. M. Chow, A. Partridge, V. Chandrasekaran, T. Nishida, M. Sheplak, C. F. Quate, T. W. Kenny, "Polysilicon Electrical Through-Wafer Interconnects For Released Silicon Sensors," to be submitted to *Journal of Microelectromechanical Systems*, 2001.

E. M. Chow, G. Yaralioglu, C. F. Quate, T. W. Kenny, "Characterization of a Two-Dimensional Cantilever Array with Through-Wafer Electrical Interconnects," submitted to *Applied Physics Letters*, 2001.

E. M. Chow, H. T. Soh, H. C. Lee, J. D. Adams, S. C. Minne, G. Yaralioglu, A. Atalar, C. F. Quate, and T. W. Kenny, "Integration of Through-Wafer Interconnects With A Two-Dimensional Cantilever Array," *Sensors and Actuators A: Physical, 83(1-3),* 118-123, 2000.

R. G. Rudnitsky, E. M. Chow, T. W. Kenny, "Rapid Biochemical Detection and Differentiation with Magnetic Force Microscope Cantilever Arrays," *Sensors and Actuators A: Physical, 83(1-3),* 256-262, 2000.

K. Y. Yasumura, T. D. Stowe, E. M. Chow, T. E. Pfafman, B. Stipe, D. Rugar, T. W. Kenny, "Quality Factors in Micron and Submicron Thick Cantilevers," *Journal of Microelectromechanical Systems,* 9 (1), 117-125, 2000.

A. Partridge, J. K. Reynolds, B. W. Chui, E. M. Chow, A. M. Fitzgerald, L. Zhang, N. I. Maluf, T. W. Kenny, "A High Performance Planar Piezoresistive Accelerometer," *Journal of Microelectromechanical Systems,* 9 (1), 58-66, 2000.

Conference Publications (Refereed)

J. A. Harley, E. M. Chow, T. W. Kenny, "Design of resonant beam transducers: An axial force probe for atomic force microscopy," *Proceedings of the 1998 ASME International Mechanical Engineering Congress and Exposition*, Anaheim, CA, USA. Micro-Electro-Mechanical Systems (MEMS) American Society of Mechanical Engineers, Dynamic Systems and Control Division (Publication) DSC, ASME, Fairfield, NJ, USA. Vol. 66, pp. 247-252, 1998.

V. Chandrasekaran, E. M. Chow, T. W. Kenny, T. Nishida, M. Sheplak, 'Through Wafer Electrical Interconnects for MEMS Sensors," *Proceedings of the 2001 ASME International Mechanical Engineering Congress and Exposition*, New York, NY, USA. Micro-Electro-Mechanical Systems (MEMS) American Society of Mechanical Engineers, submitted April 2001.

Conference Papers (Unrefereed)

C. H. Cheng, E. M. Chow, X. Jin, S. Ergun, and B. T. Khuri-Yakub, "An Efficient Electrical Addressing Method Using Through-Wafer Vias For Two-Dimensional Ultrasonic Arrays," *Ultrasonics 2000*, Puerto Rico, Oct. 23-27, 2001.

E. M. Chow, A. Partridge, C. F. Quate, and T. W. Kenny, "Through-Wafer Electrical Interconnects Compatible With Standard Semiconductor Processing," *Solid-State Sensor and Actuator Workshop*, Hilton Head, South Carolina, USA, pp. 343-346, June 5-8, 2000.

E. M. Chow, H. T. Soh, H. C. Lee, J. D. Adams, S. C. Minne, G. Yaralioglu, A. Atalar, C. F. Quate, and T. W. Kenny, "Two-dimensional cantilever arrays with integrated through-wafer interconnects," *10th International Conference on Solid-State Sensors and Actuators*, Sendai, Japan, pp. 1886-1887, June 7-10, 1999.

R. G. Rudnitsky, E. M. Chow, T. W. Kenny, "High-Speed Biochemical Screening With Magnetic Force Microscope Cantilever Arrays," *10th International Conference On Solid-State Sensors And Actuators*, Sendai, Japan, pp.706-709, June 7-10, 1999.

K. Y. Yasumura, T. D. Stowe, E. M. Chow, T. Pfafman, T. W. Kenny, D. Rugar, "A Study of Cantilever Quality Factor," *Solid-State Sensor and Actuator Workshop*, Hilton Head, South Carolina, USA, pp. 65-70, June 8-11, 1998.

E. M. Chow, H. T. Soh, A. Partridge, S. Abdollahi-Alibeik, J. P. McVittie, A. McCarthy, J. A. Harley, T. W. Kenny, and C. F. Quate, "Fabrication of high-density cantilever arrays and through-wafer interconnects," *Solid-State Sensor and Actuator Workshop*, Hilton Head, South Carolina, USA, pp. 220-224, June 8-11, 1998.

A. Partridge, J. K. Reynolds, B. W. Chui, E. M. Chow, A. M. Fitzgerald, L. Zhang, S. R. Cooper, and T. W. Kenny, "A High Performance Planar Piezoresistive Accelerometer," *Solid-State Sensor and Actuator Workshop*, Hilton Head, South Carolina, USA, pp. 59-64, June 8-11, 1998.

Patents

E.M. Chow, W.B. Martin, C. Storment, A. Armes, "Reusable Wafer Support for Semiconductor Processing," U.S Patent No. 6187134, 1999.

References

[1] A. Mason, N. Yazdi, A. V. Chavan, K. Najafi, and K. D. Wise, "A generic multielement microsystem for portable wireless applications," *Proceedings of the IEEE*, vol. 86, pp. 1733-1746, 1998.

[2] D. J. Strike, M. G. H. Meijerink, and M. KoudelkaHep, "Electronic noses : A mini-review," *Fresenius Journal of Analytical Chemistry*, vol. 364, pp. 499-505, 1999.

[3] E. R. Fossum, "Digital camera system on a chip," *IEEE Micro*, vol. 18, pp. 8-15, 1998.

[4] H. Yamada, T. Togasaki, M. Kimura, and H. Sudo, "High-Density 3D Packaging Technology for CCD Micro-Camera System Module," presented at 14th IEEE International Conference on Micro Electro Mechanical Systems, Interlaken, Switzerland, pp. 14-17, 2001.

[5] P. Vettiger, M. Despont, U. Drechsler, U. Durig, W. Haberle, M. I. Lutwyche, H. E. Rothuizen, R. Stutz, R. Widmer, and G. K. Binnig, "The "Millipede" : More than one thousand tips for future AFM data storage," *IBM Journal of Research and Development*, vol. 44, pp. 323-340, 2000.

[6] W. P. Eaton and J. H. Smith, "Micromachined pressure sensors: Review and recent developments," *Smart Materials & Structures*, vol. 6, pp. 530-539, 1997.

[7] D. L. Polla and L. F. Francis, "Processing and characterization of piezoelectric materials and integration into microelectromechanical systems," *Annual Review of Materials Science*, vol. 28, pp. 563-597, 1998.

[8] B. T. Khuri-Yakub, C.-H. Cheng, F.-L. Degertekin, S. Ergun, S. Hansen, X.-C. Jin, and O. Oralkan, "Silicon Micromachined Ultrasonic Transducers," *Japanese Journal of Applied Physics*, vol. 39, pp. 2883-2887, 2000.

[9] B. J. Kane, M. R. Cutkosky, and G. T. A. Kovacs, "A traction stress sensor array for use in high-resolution robotic tactile imaging," *Journal of Microelectromechanical Systems*, vol. 9, pp. 425-434, 2000.

[10] G. Binnig, C. F. Quate, and C. Gerber, "Atomic Force Microscope," *Physical Review Letters*, vol. 56, pp. 930-933, 1986.

[11] R. Berger, C. Gerber, H. P. Lang, and J. K. Gimzewski, "Micromechanics: A toolbox for femtoscale science: "Towards a laboratory on a tip"," *Microelectronic Engineering*, vol. 35, pp. 373-379, 1997.

[12] Z. F. Shao, J. Mou, D. M. Czajkowsky, J. Yang, and J. Y. Yuan, "Biological atomic force microscopy: What is achieved and what is needed," *Advances in Physics*, vol. 45, pp. 1-86, 1996.

[13] H. P. Lang, R. Berger, F. Battiston, J. P. Ramseyer, E. Meyer, C. Andreoli, J. Brugger, P. Vettiger, M. Despont, T. Mezzacasa, L. Scandella, H. J. Guntherodt, C. Gerber, and J. K. Gimzewski, "A chemical sensor based on a micromechanical cantilever array for the identification of gases and vapors," *Applied Physics A-Materials Science & Processing*, vol. 66, pp. S61-S64, 1998.

[14] K. Wilder, C. F. Quate, B. Singh, and D. F. Kyser, "Electron beam and scanning probe lithography: A comparison," *Journal of Vacuum Science & Technology B*, vol. 16, pp. 3864-3873, 1998.

[15] H. T. Soh, K. Wilder, A. Atalar, and C. F. Quate, "Fabrication of 100 nm pMOSFETs with hybrid AFM/STM lithography," presented at 1997 Symposium on VLSI Technology. Digest of Technical Papers (IEEE Cat. No.97CH36114), Tokyo, Japan, pp. 129-130, 1997.

[16] G. Binnig, M. Despont, U. Drechsler, W. Haberle, M. Lutwyche, P. Vettiger, H. J. Mamin, B. W. Chui, and T. W. Kenny, "Ultrahigh-density atomic force microscopy data storage with erase capability," *Applied Physics Letters*, vol. 74, pp. 1329-31, 1999.

[17] C. F. Quate, "Scanning probes as a lithography tool for nanostructures," *Surface Science*, vol. 386, pp. 259-264, 1997.

[18] S. C. Minne, S. R. Manalis, and C. F. Quate, "Parallel Atomic-Force Microscopy Using Cantilevers With Integrated Piezoresistive Sensors and Integrated Piezoelectric Actuators," *Applied Physics Letters*, vol. 67, pp. 3918-3920, 1995.

[19] E. M. Chow, H. T. Soh, H. C. Lee, J. D. Adams, S. C. Minne, G. Yaralioglu, A. Atalar, C. F. Quate, and T. W. Kenny, "Integration of through-wafer interconnects with a two-dimensional cantilever array," *Sensors and Actuators A-Physical*, vol. 83, pp. 118-123, 2000.

[20] D. W. Lee, T. Ono, T. Abe, and M. Esashi, "Fabrication of microprobe array with sub-100nm nano-heater for nanometric thermal imaging and data storage," presented at 14th IEEE International Conference on Micro Electro Mechanical Systems (MEMS2001), Interlaken, Switzerland, pp. 204-207, 2001.

[21] K. Wilder and C. F. Quate, "Scanning probe lithography using a cantilever with integrated transistor for on-chip control of the exposing current," *Journal of Vacuum Science & Technology B*, vol. 17, pp. 3256-3261, 1999.

[22] S. F. AlSarawi, D. Abbott, and P. D. Franzon, "A review of 3-D packaging technology," *IEEE Transactions On Components Packaging and Manufacturing Technology Part B-Advanced Packaging*, vol. 21, pp. 2-14, 1998.

[23] M. Heschel, J. F. Kuhmann, S. Bouwstra, and M. Amskov, "Stacking technology for a space constrained microsystem," *Journal of Intelligent Material Systems and Structures*, vol. 9, pp. 749-54, 1998.

[24] S. Linder, "Chip Stacks for Memory Applications," Ph.D. thesis from Swiss Federal Institute of Technology in Physical Electronics Laboratory, 1996.

[25] K. W. Lee, T. Nakamura, T. Ono, Y. Yamada, T. Mizukusa, and H. Hashimoto, "Three-dimensional Shared Memory Fabricated Using Wafer Stacking Technology," presented at International Electron Devices Meeting, San Fransisco, CA, pp. 165-168, 2000.

[26] N. Takahashi, N. Senba, Y. Shimada, I. Morisaki, and K. Tokuno, "Three-dimensional memory module," *IEEE Transactions On Components Packaging and Manufacturing Technology Part B-Advanced Packaging*, vol. 21, pp. 15-19, 1998.

[27] S. Souri, K. Banerjee, A. Mehrotra, and K. Saraswat, "Multiple Si Layer ICs: Motivation, Performance Analysis, and Design Implications," presented at 37th Design Automation Conference, Proceedings 2000, pp. 213-220, 2000.

[28] S. K. Bhattacharya, J. Y. Park, R. R. Tummala, and M. G. Allen, "Fabrication of a fully integrated passive module for filter application using MCM-D compatible processes," *Journal of Materials Science-Materials in Electronics*, vol. 11, pp. 455-460, 2000.

[29] R. G. Arnold, C. C. Faulkner, and D. J. Pedder, "Silicon MCM-D technology for RF integration," *GEC Journal of Technology*, vol. 14, pp. 85-89, 1997.

[30] J. Hartung, "Integrated Passive Components in MCM-Si Technology and their Applications in RF-Systems," presented at 1998 7th International Conference on Multichip Modules and High Density Packaging, Denver, CO, pp. 256-261, 1998.

[31] J. H. Wu, J. A. del Alamo, and K. A. Jenkins, "A High Aspect-Ratio Silicon Substrate-Via Technology and Applications: Through-Wafer Interconnects for Power and Ground and Faraday Cages for SOC Isolation," presented at International Electron Devices Meeting, San Fransisco, CA, pp. 477-480, 2000.

[32] H. Furukawa, T. Fukui, T. Tanaka, A. Noma, and D. Ueda, "A Novel Fabrication Process of Surface Via-Holes for GaAs Power FETS," presented at 20th Annual Gallium Arsenide Integrated Circuit Symposium Technical Digest, pp. 251-254, 1998.

[33] X. C. Jin, S. Calmes, C. H. Cheng, F. L. Degertekin, and B. T. Khuri-Yakub, "Micromachined capacitive ultrasonic immersion transducer array," presented at 10th International Conference on Solid-State Sensors and Actuators (Transducers '99), Sendai, Japan, pp. 1500-1503, 1999.

[34] C. H. Mastrangelo, M. A. Burns, and D. T. Burke, "Microfabricated devices for genetic diagnostics," *Proceedings of the IEEE*, vol. 86, pp. 1769-1787, 1998.

[35] H. T. Soh, C. P. Yue, A. McCarthy, C. Ryu, T. H. Lee, S. S. Wong, and C. F. Quate, "Ultra-low resistance, through-wafer via (TWV) technology and its applications in three dimensional structures on silicon," *Japanese Journal of Applied Physics, Part 1 (Regular Papers, Short Notes & Review Papers)*, vol. 38, pp. 2393-6, 1999.

[36] C. Kenney, S. Parker, J. Segal, and C. Storment, "Silicon detectors with 3-D electrode arrays: fabrication and initial test results," *IEEE Transactions on Nuclear Science*, vol. 46, pp. 1224-36, 1999.

[37] H. Baltes, "CMOS micro electro mechanical systems," *Sensors and Materials*, vol. 9, pp. 331-346, 1997.

[38] K. A. Honer and G. T. A. Kovacs, "Sputtered Silicon for Integrated MEMS Applications," presented at Solid-State Sensor and Actuator Workshop, Hilton Head Island, South Carolina, pp. 308-311, 2000.

[39] J. J. Sniegowski and M. P. deBoer, "IC-compatible polysilicon surface micromachining," *Annual Review of Materials Science*, vol. 30, pp. 299-333, 2000.

[40] D. J. Bartelink, "Integrated systems," *IEEE Transactions On Electron Devices*, vol. 43, pp. 1678-1687, 1996.

[41] J. T. Butler, V. M. Bright, P. B. Chu, and R. J. Saia, "Adapting Multichip Module Foundries for MEMS Packaging," presented at 1998 7th International Conference on Multichip Modules and High Density Packaging, Denver, CO, pp. 106-111, 1998.

[42] Y. Murakami and B. B. Mikic, "Parametric optimization of multichanneled heat sinks for VLSI chip cooling," *IEEE Transactions On Components and Packaging Technologies*, vol. 24, pp. 2-9, 2001.

[43] D. Hulsenberg, "Glasses for microsystems technology," *Microelectronics Journal*, vol. 28, pp. 419-432, 1997.

[44] P. F. Indermuhle, E. Ammann, P. Haring, R. Kotz, H. Siegenthaler, and N. F. deRooij, "Electrolytic thin layer scanning tunneling microscope: fabrication and first results," *Microelectronic Engineering*, vol. 42, pp. 547-550, 1998.

[45] X. Li, T. Abe, Y. Liu, and M. Esashi, "High Density Electrical Feedthrough Fabricated by Deep Reactive Ion Etching of Pyrex Glass," presented at 14th IEEE International Conference on Micro Electro Mechanical Systems, Interlaken, Switzerland, pp. 98-101, 2001.

[46] T. R. Anthony, "Forming electrical interconnections through semiconductor wafers," *Journal of Applied Physics*, vol. 52, pp. 5340-9, 1981.

[47] C. H. Cheng, E. M. Chow, X. Jin, S. Ergun, and B. T. Khuri-Yakub, "An Efficient Electrical Addressing Method Using Through-Wafer Vias for Two-Dimensional Ultrasonic Arrays," presented at 2000 IEEE International Ultrasonics Symposium, San Juan, Puerto Rico, pp. 1179 -1182, 2000.

[48] C. Christensen, P. Kersten, S. Henke, and S. Bouwstra, "Wafer through-hole interconnections with high vertical wiring densities," *IEEE Transactions on Components, Packaging, and Manufacturing Technology, Part A*, vol. 19, pp. 516-22, 1996.

[49] S. Linder, H. Baltes, F. Gnaedinger, and E. Doering, "Fabrication technology for wafer through-hole interconnections and three-dimensional stacks of chips and wafers," presented at Proceedings IEEE Micro Electro Mechanical Systems. An

Investigation of Micro Structures, Sensors, Actuators, Machines and Robotic Systems (Cat. No.94CH3404-1), New York, NY, USA, pp. 349-354, 1994.

[50] G. J. Burger, E. J. T. Smulders, J. W. Berenschot, T. S. J. Lammerink, J. H. J. Fluitman, and S. Imai, "High-resolution shadow-mask patterning in deep holes and its application to an electrical wafer feed-through," *Sensors and Actuators A-Physical*, vol. 54, pp. 669-673, 1996.

[51] S. Savastiouk, "Moore's Law : the z dimension," *Solid State Technology*, vol. 43, pp. 84, 2000.

[52] A. Mehra, X. Zhang, A. A. Ayon, I. A. Waitz, and M. A. Schmidt, "Through-wafer electrical interconnect for multilevel microelectromechanical system devices," *Journal of Vacuum Science & Technology B*, vol. 18, pp. 2583-2589, 2000.

[53] N. P. Pham, K. T. Ng, M. Bartek, P. M. Sarro, B. Rejaei, and J. N. Burghartz, "A Micromachining Post-Process Module for RF Silicon Technology," presented at International Electron Devices Meeting, San Fransisco, CA, pp. 481-484, 2000.

[54] K. M. Strohm, P. Nuechter, C. N. Rheinfelder, and R. Guehl, "Via Hole Technology For Microstrip Transmission Lines And Passive Elements on High Resistivity Silicon," presented at IEEE MTT-S International Microwave Symposium, Aneheim, CA, pp. 581-584, 1999.

[55] J. Bhardwaj, H. Ashraf, A. McQuarrie, G. Barna, and H. G. Hughes, "Dry silicon etching for MEMS," presented at Proceedings of the Third International Symposium on Microstructures and Microfabricated Systems, Pennington, NJ, USA, pp. 118-130, 1997.

[56] M. J. Madou, *Fundamentals of Microfabrication*. Boca Raton, Florida: CRC, 1997.

[57] S. Ottow, V. Lehmann, and H. Foll, "Development of three-dimensional microstructure processing using macroporous n-type silicon," *Applied Physics a-Materials Science & Processing*, vol. 63, pp. 153-159, 1996.

[58] S. S. Cahill, W. Chu, and K. Ikeda, "High Aspect Ratio Isolated Structures in Single Crystal Silicon," presented at 7th International Conference on Solid-State Sensors and Actuators (Tranducers '93), Yokohama, Japan, pp. 250-253, 1993.

[59] V. Lehmann, "Porous Silicon - A new Material for MEMS," presented at 9th IEEE International Workshop on Micro Electro Mechanical Systems, San Diego, CA, pp. 1-6, 1996.

[60] F. Laermer and A. Schilp, "Method of anisotropically etching silicon," U.S. Patent No. 5501893, 1996.

[61] E. H. Klaassen, K. Petersen, J. M. Noworolski, J. Logan, N. I. Maluf, J. Brown, C. Storment, W. McCulley, and G. T. A. Kovacs, "Silicon fusion bonding and deep reactive ion etching: A new technology for microstructures," *Sensors and Actuators A-Physical*, vol. 52, pp. 132-139, 1996.

[62] A. A. Ayon, R. Braff, C. C. Lin, H. H. Sawin, and M. A. Schmidt, "Characterization of a time multiplexed inductively coupled plasma etcher," *Journal of the Electrochemical Society*, vol. 146, pp. 339-49, 1999.

[63] R. J. Shul and J. G. Fleming, "Bulk Si Micromachining for Integrated Microsystems and MEMS Processing," in *Handbook of Advanced Plasma Processing Techniques*, R. J. Shul and S. J. Pearton, Eds.: Springer-Verlag, 2000, pp. 419-458.

[64] H. J. Jansen, M. d. Boer, and M. Elwenspoek, "The Black Silicon Method VI: High Aspect Ratio Trench Etching For MEMS Applications," presented at 9th Annual International Workshop on Micro Electro Mechanical Systems, San Diego, CA, pp. 250-257, 1996.

[65] T. Kinoshita, M. Hane, and J. P. McVittie, "Notching as an example of charging in uniform high density plasmas," *Journal of Vacuum Science & Technology B*, vol. 14, pp. 560-565, 1996.

[66] A. A. Ayon, K. Ishihara, R. A. Braff, H. H. Sawin, and M. A. Schmidt, "Application of the footing effect in the micromachining of self-aligned, free-standing, complimentary metal-oxide-semiconductor compatible structures," *Journal of Vacuum Science & Technology A-Vacuum Surfaces and Films*, vol. 17, pp. 2274-2279, 1999.

[67] A. M. Hynes, H. Ashraf, J. K. Bhardwaj, J. Hopkins, I. Johnston, and J. N. Shepherd, "Recent advances in silicon etching for MEMS using the ASE(TM) process," *Sensors and Actuators A-Physical*, vol. 74, pp. 13-17, 1999.

[68] H. Ashraf, J. K. Bhardwaj, S. Hall, J. Hopkins, A. M. Hynes, I. Johnston, S. McAuley, G. Nicholls, L. Atabo, M. E. Ryan, and S. C. Watcham, "Advances In Deep Anisotropic Silicon Etch Processing For MEMS," presented at 5th National Conference On Sensors And Microsystems, The Italian Association of Sensors and Microsystems, Lecce, Italy, 2000.

[69] H. Ashraf, J. K. Bhardwaj, S. Hall, E.Guibarra, and J. Hopkins, "Defining Conditions for the Etching of Silicon In An Inductive Coupled Plasma Reactor," presented at Materials Research Society Fall Meeting, Boston, Massachusetts, USA, 1999.

[70] www.stsystems.com, Surface Technology Systems Quarterly News Bulletin, March, 1999.

[71] T. D. Stowe, K. Yasumura, T. W. Kenny, D. Botkin, K. Wago, and D. Rugar, "Attonewton force detection using ultrathin silicon cantilevers," *Applied Physics Letters*, vol. 71, pp. 288-290, 1997.

[72] E. M. Chow, H. T. Soh, A. Partridge, J. A. Harley, T. W. Kenny, C. F. Quate, S. Abdollahi-Alibeik, J. P. McVittie, and A. McCarthy, "Fabrication of high-density cantilever arrays and through-wafer interconnects," presented at Solid-State Sensor and Actuator Workshop, Hilton Head Island, pp. 220-224, 1998.

[73] Y. I. Lee, K. H. Park, J. Lee, C. S. Lee, H. J. Yoo, C. J. Kim, and Y. S. Yoon, "Dry release for surface micromachining with HF vapor-phase etching," *Journal of Microelectromechanical Systems*, vol. 6, pp. 226-33, 1997.

[74] G. S. Oehrlein, *Handbook of plasma processing technology*. New Jersey: Noyes Publications, 1990.

[75] J. B. Carter, J. P. Holland, E. Peltzer, B. Richardson, E. Bogle, H. T. Nguyen, Y. Melaku, D. Gates, and M. Ben-Dor, "Transformer coupled plasma etch technology for the fabrication of subhalf micron structures," *Journal of Vacuum Science & Technology A (Vacuum, Surfaces, and Films)*, 1993.

[76] E. M. Chow, W. Martin, C. Storment, and A. Armes, "Reusable Wafer Support for Semiconductor Processing," U.S. Patent No. 6187134, 1999.

[77] S. C. Minne, J. D. Adams, G. Yaralioglu, S. R. Manalis, A. Atalar, and C. F. Quate, "Centimeter scale atomic force microscope imaging and lithography," *Applied Physics Letters*, vol. 73, pp. 1742-1744, 1998.

[78] M. Lutwyche, C. Andreoli, G. Binnig, J. Brugger, U. Drechsler, W. Haberle, H. Rohrer, H. Rothuizen, P. Vettiger, G. Yaralioglu, and C. Quate, "5x5 2D AFM cantilever arrays a first step towards a Terabit storage device," *Sens. Actuators A, Phys. (Switzerland), Sensors and Actuators A (Physical)*, vol. A73, pp. 89-94, 1999.

[79] H. P. Lang, R. Berger, C. Andreoli, J. Brugger, M. Despont, P. Vettiger, C. Gerber, J. K. Gimzewski, J. P. Ramseyer, E. Meyer, and H. J. Guntherodt, "Sequential position readout from arrays of micromechanical cantilever sensors," *Applied Physics Letters*, vol. 72, pp. 383-385, 1998.

[80] J. A. Harley and T. W. Kenny, "1/f noise considerations for the design and process optimization of piezoresistive cantilevers," *Journal of Microelectromechanical Systems*, vol. 9, pp. 226-235, 2000.

[81] A. Boisen, O. Hansen, and S. Bouwstra, "AFM probes with directly fabricated tips," *Journal of Micromechanics and Microengineering*, pp. 58-62, 1996.

[82] I. W. Rangelow, "Sharp silicon tips for AFM and field emission," *Microelectronic Engineering*, vol. 23, pp. 369-372, 1994.

[83] J. Itoh, Y. Tohma, S. Kanemaru, and K. Shimizu, "Fabrication of an ultrasharp microprobe with a silicon-on-insulator wafer for scanning force microscopy," *Journal of Vacuum Science and Technology B*, vol. 13, pp. 331-334, 1995.

[84] R. B Marcus, T. S. Ravi, T. Gmitter, K. Chin, D. Liu, W. J. Orvis, D. R. Ciarlo, C. E. Hunt, and J. Trujillo, "Formation of silicon tips with <1 nm radius," *Applied Physics Letters*, vol. 56, pp. 237-238, 1990.

[85] J. Thaysen, A. Boisen, O. Hansen, and S. Bouwstra, "AFM Probe With Piezoresistive Read-out And Highly Symmetrical Wheatstone Bridge Arrangement," presented at 10th International Conference on Solid-State Sensors and Actuators (Transducers '99), Sendai, Japan, pp. 1852-1855, 1999.

[86] M. Tortonese, "Force Sensors for Scanning Probe Microscopy," Ph.D. thesis from Stanford University in Applied Physics, 1993.

[87] Y. Kanda, "A Graphical Representation of the Piezoresistance Coefficients in Silicon," *IEEE Transactions On Electron Devices*, vol. 29, pp. 64-70, 1982.

[88] C. Ciofi and B. Neri, "Low-frequency noise measurements as a characterization tool for degradation phenomena in solid-state devices," *Journal of Physics D-Applied Physics*, vol. 33, pp. R199-R216, 2000.

[89] R. P. Ried, J. Mamin, B. D. Terris, L. S. Fan, and D. Rugar, "6-MHz 2-N/m piezoresistive atomic-force-microscope cantilevers with INCISIVE tips," *Journal of Microelectromechanical Systems*, vol. 6, pp. 294-302, 1997.

[90] B. W. Chui, T. D. Stowe, T. W. Kenny, H. J. Mamin, B. D. Terris, and D. Rugar, "Low-stiffness silicon cantilevers for thermal writing and piezoresistive readback with the atomic force microscope," *Applied Physics Letters*, vol. 69, pp. 2767-9, 1996.

[91] S. Bhardwaj, "Noise Measurements in Silicon Piezoresistors for S/N Optimization of Piezoresistive MEMS Microphones," M.S. thesis from University of Florida in Aeronautical Engineering, 2001.

[92] G. G. Yaralioglu, "Noise Analysis of Interdigital Cantilevers For Atomic Force Microscopy," Ph.D. thesis from Bilkent University, Turkey in Electrical and Electronics Engineering, 1998.

[93] B. Bhushan and S. Sundararajan, "Micro/nanoscale friction and wear mechanisms of thin films using atomic force and friction force microscopy," *Acta Materialia*, vol. 46, pp. 3793-3804, 1998.

[94] T. Kamins, *Polycrystalline Silicon For Integrated Circuits and Displays*, 2nd ed. Boston: Kluwer Academic Publishers, 1998.

[95] D. Griffiths, *Introduction to Electrodynamics*, 2nd ed: Prentice Hall, 1989.

[96] R. A. Gottscho, C. W. Jurgensen, and D. J. Vitkavage, "Microscopic uniformity in plasma etching," *Journal of Vacuum Science & Technology B (Microelectronics and Nanometer Structures)*, vol. 10, pp. 2133-2147, 1992.

[97] E. M. Chow, A. Partridge, C. F. Quate, and T. W. Kenny, "Through-Wafer Electrical Interconnects Compatible With Standard Semiconductor Processing," presented at Solid-State Sensor and Actuator Workshop, Hilton Head Island, South Carolina, pp. 343-346, 2000.

[98] M. Y. Luo and G. Bosman, "An analytical model for 1/f noise in polycrystalline silicon thin films," *IEEE Transactions on Electron Devices*, vol. 37, pp. 768-74, 1990.

[99] M. J. Deen, S. Rumyantsev, and J. Orchard-Webb, "Low frequency noise in heavily doped polysilicon thin film resistors," *Journal of Vacuum Science & Technology B (Microelectronics and Nanometer Structures)*, vol. 16, pp. 1881-4, 1998.

[100] J. D. Plummer, M. D. Deal, and P. B. Griffin, *Silicon VLSI Technology: fundamentals, practice, and modeling*. Upper Saddle River, NJ: Prentice Hall, 2000.

[101] E. H. Nicollian and J. R. Brews, *MOS (metal oxide semicondutor) Physics and Technology*. New York: Wiley, 1982.

[102] S. Wolf and R. N. Tauber, *Silicon Processing for the VLSI Era - Process Technology*, vol. 1. Sunset Beach: Lattice Press, 1986.

[103] V. Chandrasekaran, E. M. Chow, T. W. Kenny, T. Nishida, and M. Sheplak, "Through-Wafer Electrical Interconnects for MEMS Sensors," presented at Proceedings of the 2001 ASME International Mechanical Engineering Congress and Exposition, New York, NY, 2001.

[104] J. Kiihamaki, "Deceleration of silicon etch rate at high aspect ratios," *Journal of Vacuum Science & Technology A-Vacuum Surfaces and Films*, vol. 18, pp. 1385-1389, 2000.

[105] V. A. Yunkin, V. F. Lukichev, K. V. Rudenko, D. Fischer, and E. Voges, "Experimental study and computer simulation of aspect ratio dependent effects observed in silicon reactive ion etching," *Microelectronic Engineering*, vol. 30, pp. 345-348, 1996.

[106] H. Treichel, A. Mitwalsky, N. P. Sandler, D. Tribula, W. Kern, and A. P. Lane, "Low-pressure chemical vapour deposition of tantalum pentoxide films for ULSI devices using tantalum pentaethoxide as precursor," *Advanced Materials for Optics and Electronics*, vol. 1, pp. 299-308, 1992.

[107] S. Duenas, E. Castan, J. Barbolla, R. R. Kola, and P. A. Sullivan, "Use of anodic tantalum pentoxide for high-density capacitor fabrication," *Journal of Materials Science-Materials in Electronics*, vol. 10, pp. 379-384, 1999.

[108] V. Subramanian and K. C. Saraswat, "High-performance germanium-seeded laterally crystallized TFT's for vertical device integration," *IEEE Transactions On Electron Devices*, vol. 45, pp. 1934-1939, 1998.

[109] A. E. Franke, Y. Jiao, M. T. Wu, T. J. King, and R. T. Howe, "Post-Cmos Modular Integration of Poly-SiGe Microstructures Using Poly-Ge Sacrificial Layers," presented at Solid-State Sensor and Actuator Workshop, Hilton Head Island, South Carolina, pp. 18-21, 2000.

[110] X. Y. Chen and C. Salm, "Doping dependence of low-frequency noise in polycrystalline SiGe film resistors," *Applied Physics Letters*, vol. 75, pp. 516-518, 1999.

[111] M. Furtsch, "Mechanical Properties of Thick Polycrystalline Silicon Films Suitable for Surface Micromachining," Ph.D. thesis from in Mechanical Engineering, 1999.

[112] J. M. Drynan, E. Ikawa, and T. Kikkawa, "Fabrication of polysilicon plugs for deep-submicron contact-holes," presented at 1990 Proceedings. Seventh International IEEE VLSI Multilevel Interconnection Conference (Cat. No.90TH0325-1), New York, NY, USA, pp. 494, 1990.

[113] T. Hamajima and Y. Sugano, "Low contact resistance polysilicon plug for halfmicron CMOS technology," presented at 1989 Proceedings. Sixth International IEEE VLSI Multilevel Interconnection Conference (Cat. No.89TH0259-2), New York, NY, USA, pp. 508, 1989.

[114] D. Chidambarrao, J. P. Peng, and G. R. Srinivasa, "Stresses in silicon substrates near isolation trenches," *Journal of Applied Physics*, vol. 70, pp. 4816-22, 1991.